ADC EXTENDED I/O BITS 49 – 80

	BIT	PIN	I/O	SIGNAL	FUNCTION	TO
BLOCK 6, BANK 4		44		I/OC49–56	+5V*	–
		43		OUTC49–56	–	–
	49	42	I	2RET (FWD_RET_2ND)	FWD CELL RETRACT 2ND LIMIT	J702–6
	50	41	I	2DPL (FWD_DEP_2ND)	FWD CELL DEPLOY 2ND LIMIT	J702–7
	51	40	I	AFT_RET_2ND	AFT CELL RETRACT 2ND LIMIT	J701–10
	52	39	I	AFT_DEP_2ND	AFT CELL DEPLOY 2ND LIMIT	J701–11
	53	38	I	AFT_HOME	AFT CELL HOME FIDUCIAL	J701–12
	54	37	I	–	–	–
	55	36	I	–	–	–
	56	35	I	–	–	–
BLOCK 7, BANK 5		34		I/OC57–64	+5V*	–
		33		OUTC57–64	–	–
	57	32	I	$\overline{\text{MOTOR\_CONN}}$	MOTOR CABLE CONNECTED	J702–8
	58	31	I	$\overline{\text{MOTOR\_ENCD\_CONN}}$	MOTOR ENCODER CABLE CONNECTED	J701–15
	59	30	I	$\overline{\text{LOAD\_ENCD\_CONN}}$	LOAD ENCODER CABLE CONNECTED	J701–16
	60	29	I	$\overline{\text{FWD\_CELL\_CONN}}$	FORWARD CELL LIMIT CABLE CONNECTED	J701–17
	61	28	I	$\overline{\text{AFT\_CELL\_CONN}}$	AFT CELL LIMIT CABLE CONNECTED	J701–18
	62	27	I	$\overline{\text{MAN\_PADDLE\_CONN}}$	LOW WHEN PADDLE IS CONNECTED	J702–9
	63	26	I	$\overline{\text{MAIN\_CABLE\_CONN}}$	MAIN LOGIC CABLE IS CONNECTED	J701–2
	64	25	I	–	–	–

	BIT	PIN	I/O	SIGNAL	FUNCTION	TO
BLOCK 8, BANK 6		24		I/OC65–72	+5V*	–
		23		OUTC65–72	–	–
	65	22	I	E–STOP	OBSERVATORY E–STOP INPUT SIGNAL	J702–11
	66	21	I	EMERGENCY_STOP	EMERGENCY STOP BUTTON PUSHED	J702–5
	67	20	I	LOCAL/$\overline{\text{REMOTE}}$	INSTRUMENT CONTROL SWITCH INPUT	J702–12
	68	19	I	BYPASS_MODE	EMERGENCY NULL MODE IN EFFECT	J702–13
	69	18	I	–	–	–
	70	17	I	–	–	–
	71	16	I	–	–	–
	72	15	I	–	–	–
BLOCK 9, BANK 7		14		I/OC73–80	+5V*	–
		13		OUTC73–80	–	–
	73	12	I	–	–	–
	74	11	I	–	–	–
	75	10	I	–	–	–
	76	9	I	–	–	–
	77	8	I	–	–	–
	78	7	I	–	–	–
	79	6	I	–	–	–
	80	5	I	–	–	–
		4		+5V	+5V DC OUT FROM J1	–
		3		GND	GROUND PINS OF J1	J701–1, 7, 9, 13
		2		+5V	+5V DC OUT FROM J1	J701–8
		1		GND	GROUND PINS OF J1	J702–1, 4, 12, 20, 21

*+5V IS DAISY CHAINED FROM TERMINALS 2 AND 4.

NOTES: 1) I/O BIT NUMBERS STARTING WITH A 'P' DENOTE POWER DRIVER ABILITY

2) AS PER GALIL APP. NOTE #1438, TO USE BANKS 0 AND 1 FOR INPUTS, THE IOM–1964 CONNECTION LABELED OUTCn MUST BE CONNECTED TO THE ISOLATED POWER SUPPLY GROUND.

B

REVISIONS

03–05–04 ADDED $\overline{\text{FLOW\_OK}}$ AND $\overline{\text{FLOW\_CONN}}$ INPUTS
04–26–04 CHANGED LABELS FOR SECONDARY LIMITS – AT STAGE THEY ARE $\overline{\text{FWD\_RET\_2ND}}$ AND $\overline{\text{FWD\_DEP\_2ND}}$ AFTER INTERLOCKS THAY ARE $\overline{\text{2RET}}$ AND $\overline{\text{2DPL}}$
05–05–04 CHANGED E–STOP AND EMERGENCY STOP TO HIGH TRUE LOGIC AND RENAMED LOCAL/REMOTE SWITCH
05–27–04 REMOVED EMERGENCY NULL PADDLE INPUTS AT BITS 62 AND 63 AND ADDED EMERGENCY NULL MODE INPUT AT BIT 68
06–15–04 REWORKED FOR MANUAL PADDLE WIRING
10–13–04 ADDED I/O– AND OUT– COMMON PINS. ADDED PINS 1–4
10–25–04 CORRECTED GND CONNECTIONS AT PINS 1 AND 3 AND REMOVED +5V CONNECTION (5v COMES FROM AMP–19520)
02–07–05 CORRECTED SIGNAL CONNECTIONS FROM J405 TO J701 (J701 IS THE CONNECTOR ON THE I/O PANEL AND J405 IS ON THE INTERLOCK PANEL)
03–12–07 CHANGE LOCAL/REMOTE LABLE TO LOCAL/REMOTE FOR I/O BIT 67

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

ADC EXTENDED I/O
SIGNALS AND WIRING
KECK ADC

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