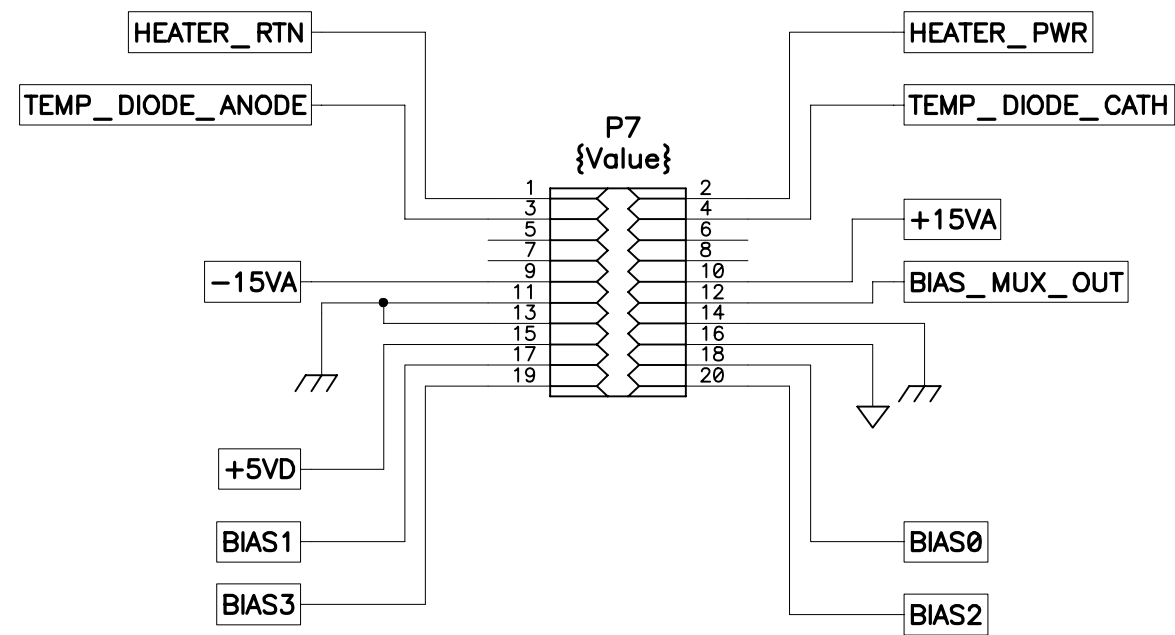
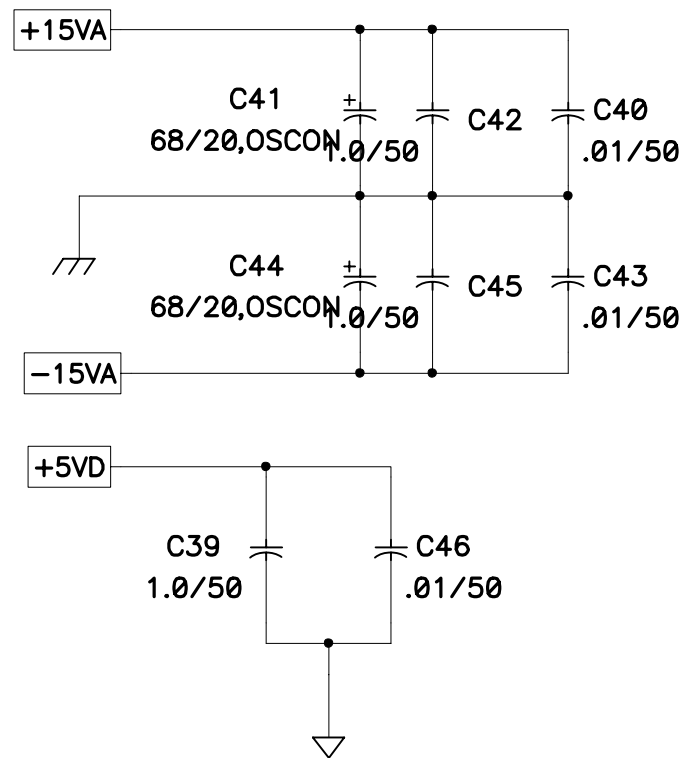



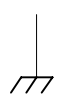

INPUT/OUTPUT/POWER CONNECTOR  
FROM UTILITY SUPPORT BOARD



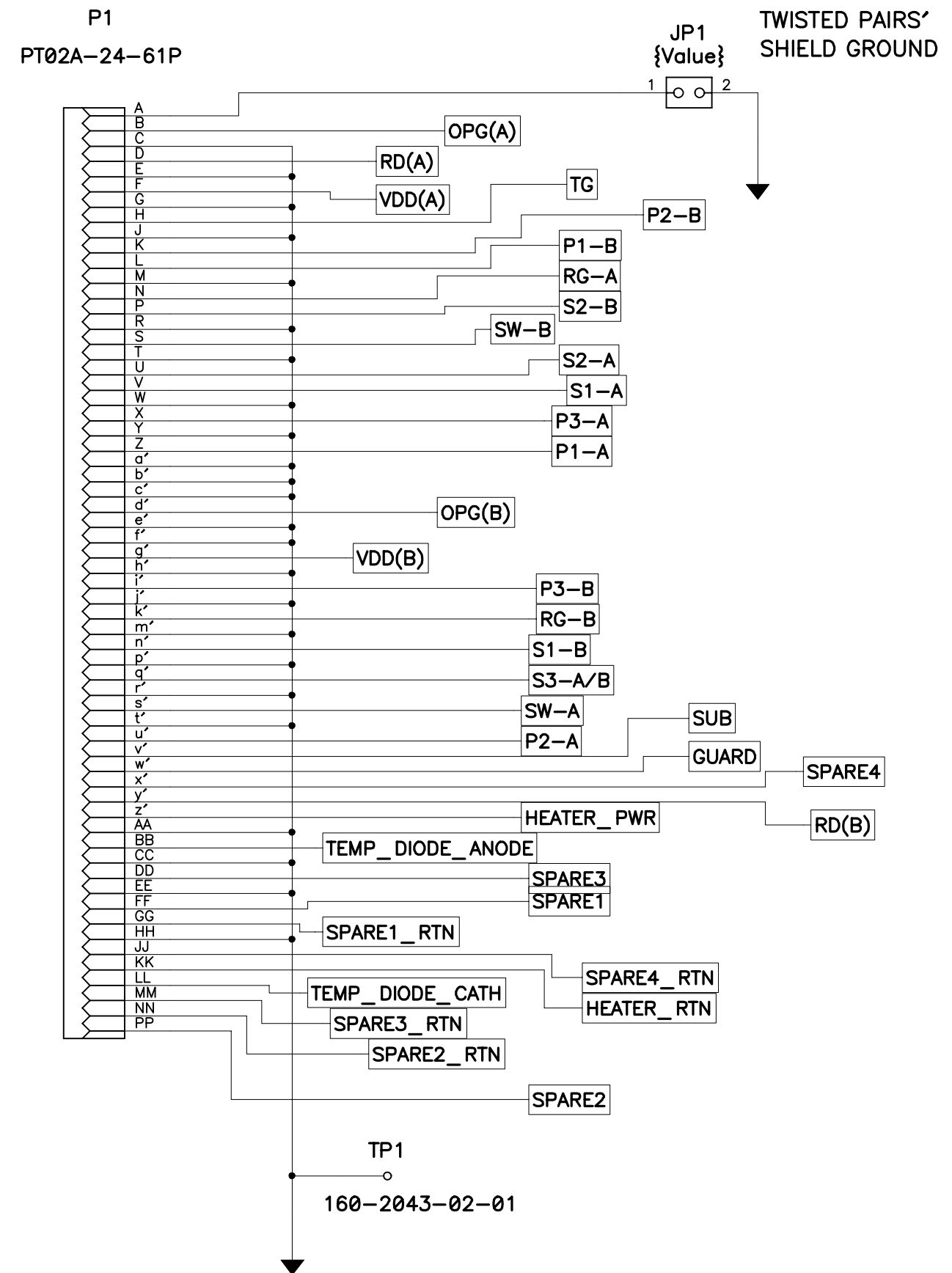
POWER FILTERS



NOTE: THE FOLLOWING GROUND SYMBOLS ARE USED:

- 
 CCD SIGNAL GROUND  
(BOTH CLOCK DRIVER BRD & VIDEO PROCESSING BRD  
INPUT GROUNDS TIED TOGETHER)
- 
 +/- 15VA GROUND (FROM UTILITY SUPPORT BRD)
- 
 +5VD GROUND (FROM UTILITY SUPPORT BRD)

OUTPUT CONNECTOR TO ELECTRONICS BOX



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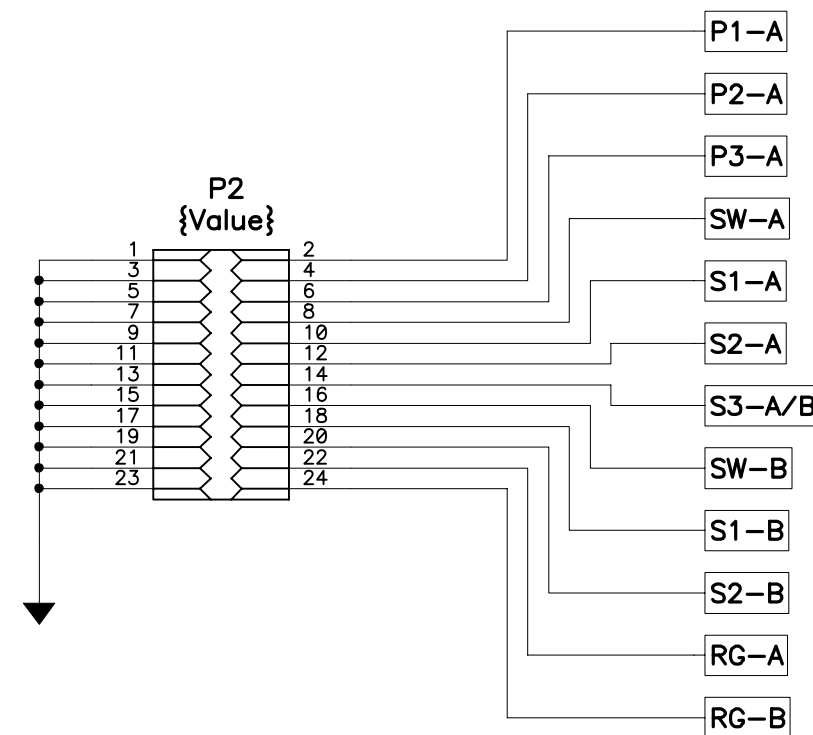
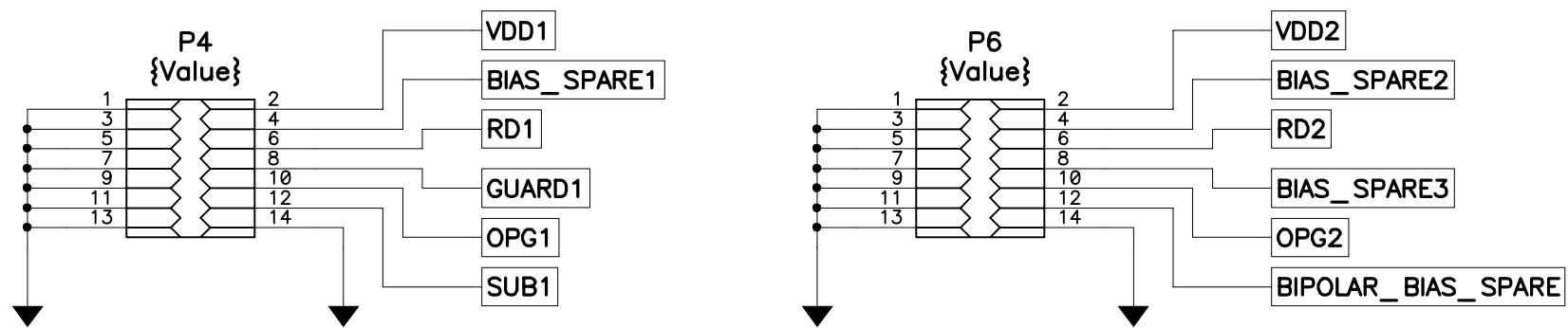
UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	
61-PIN CABLE INTERCONNECT	
DWG. NO.	EL-3194
DES'N BY: Chris Wright	ORIGIN DATE: APRIL 20, 1998
DRAWN BY:	MODIFY DATE:
PATH: sdsuccd2\boards\el3194\cblconn.sch	SHEET 1 OF 5

BIAS VOLTAGES – FROM SDSU-2 VIDEO BRD  
(VIA BIAS CABLE INTERCONNECT BRD)

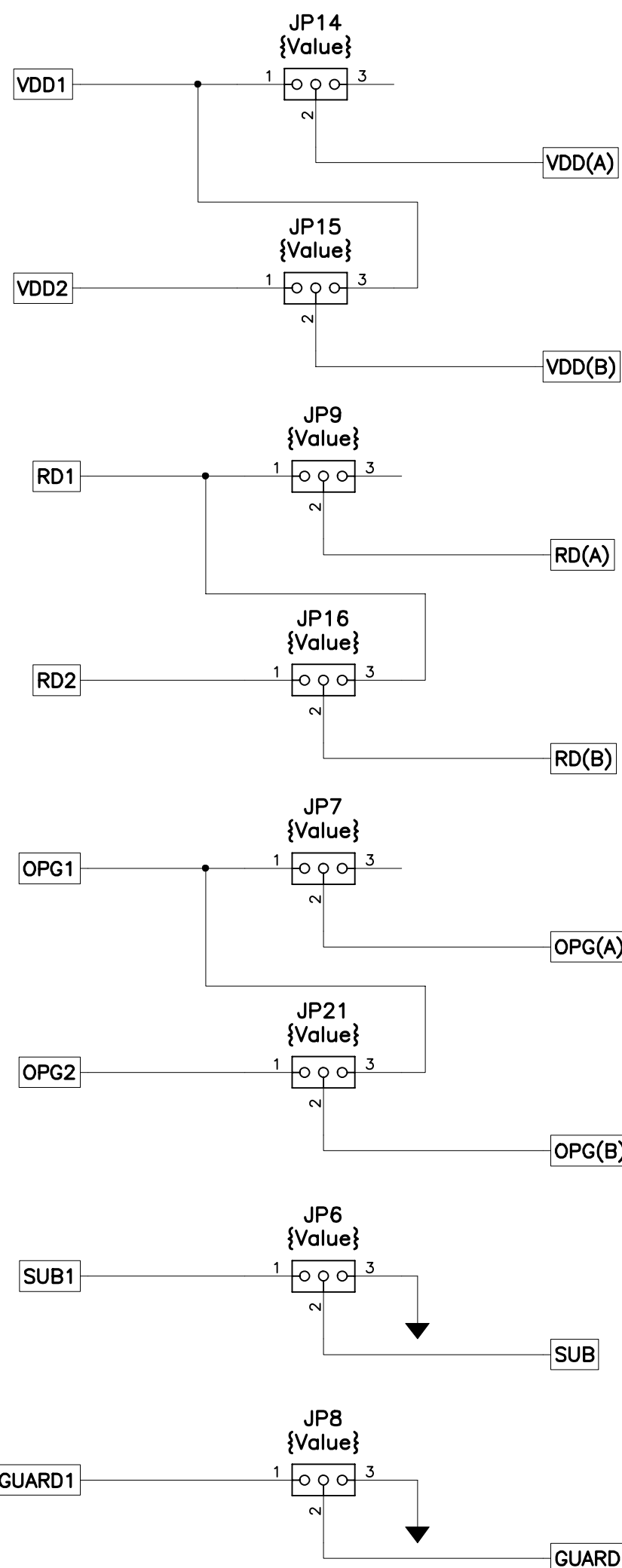
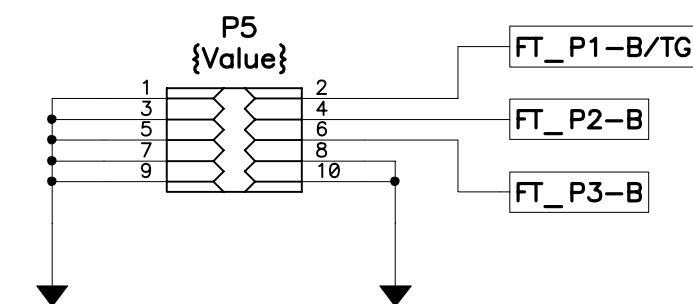
CLOCKS – FROM SDSU-2 CLOCK DRIVER BRD  
(VIA CLOCK CABLE INTERCONNECT BRD #1)

CLOCKS – FROM SDSU-2 CLOCK DRIVER BRD  
(VIA CLOCK CABLE INTERCONNECT BRD #2)

ONLY CONNECTED FOR  
DUAL READOUT ON CCD

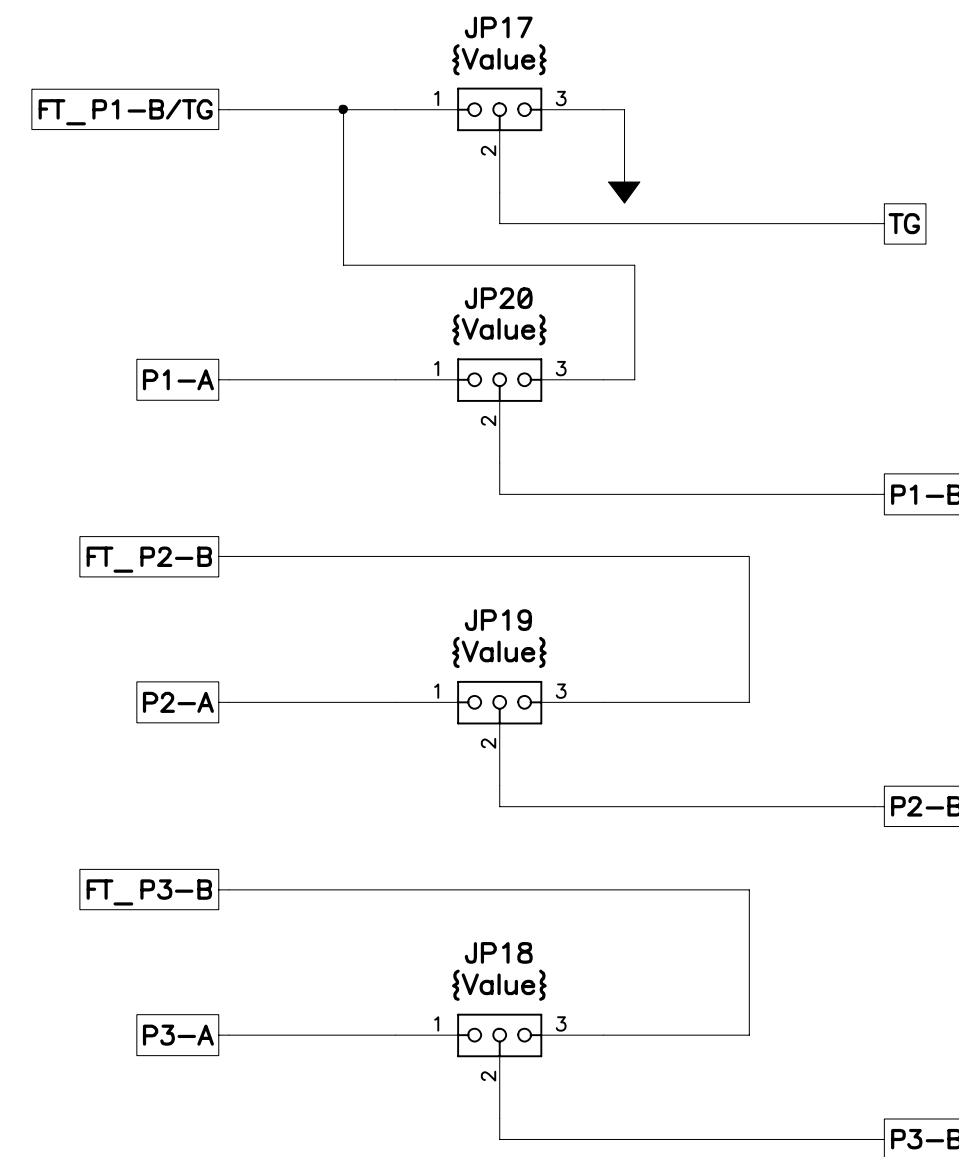


USED FOR FRAME TRANSFER  
OR 'TG' CLOCKS



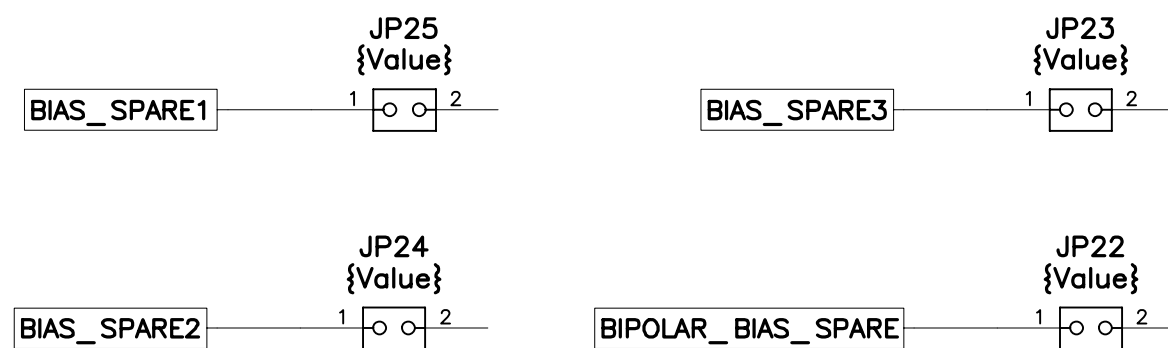
BIAS  
OUTPUTS

**NOTE:** SEE PAGE 5 FOR  
JUMPER COMBINATIONS  
OF PARTICULAR CCDs &  
SYSTEM CONFIGURATIONS.



OUTPUT  
CLOCKS

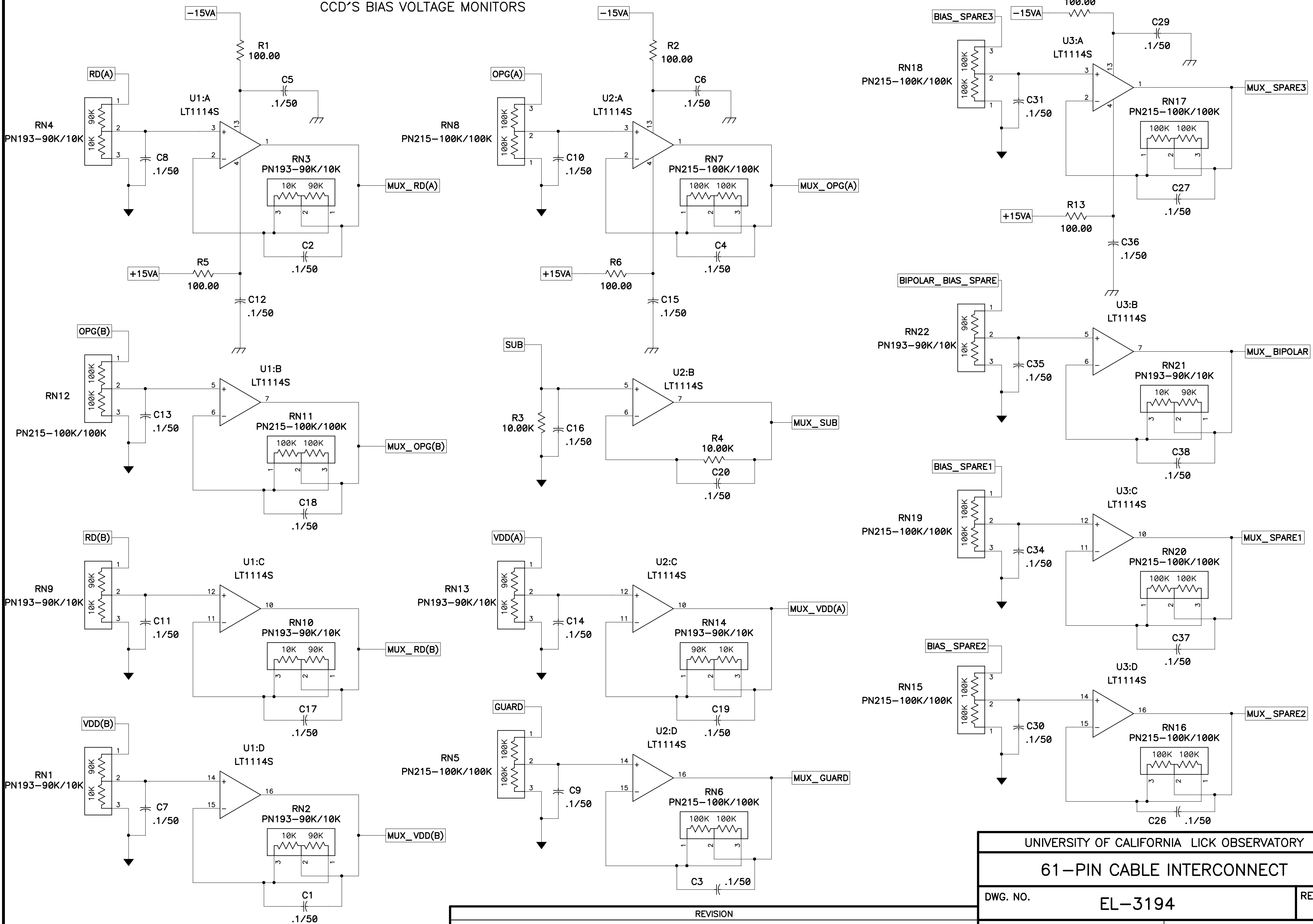
SPARE BIAS VOLTAGES



UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		
61-PIN CABLE INTERCONNECT		
DWG. NO.	EL-3194	REV B
DES'N BY: Chris Wright	ORIGIN DATE: APRIL 20, 1998	
DRAWN BY:	MODIFY DATE:	
PATH: sdsuccd2\boards\el3194\cblconn.sch	SHEET 2 OF 5	

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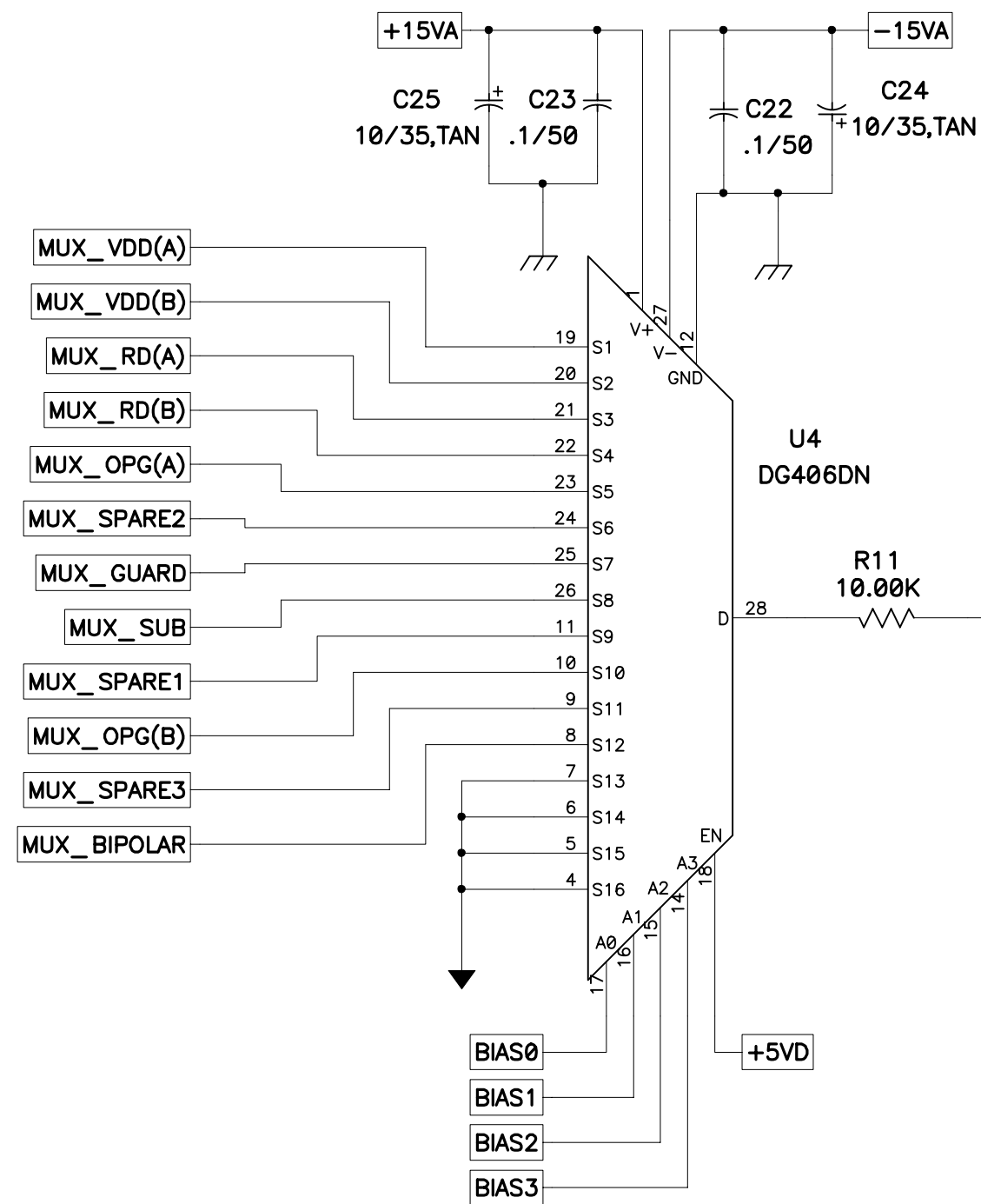
CCD'S BIAS VOLTAGE MONITORS



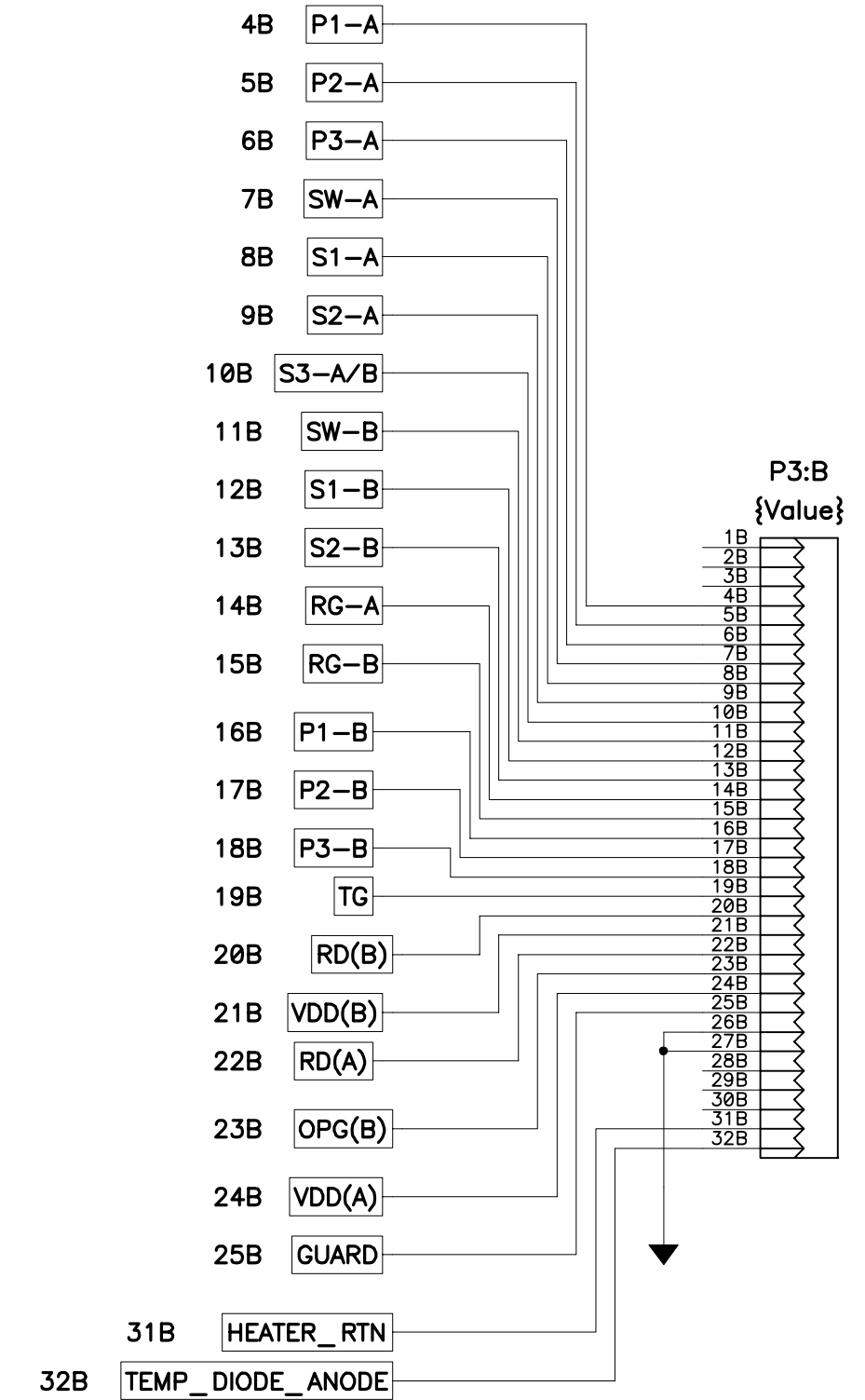
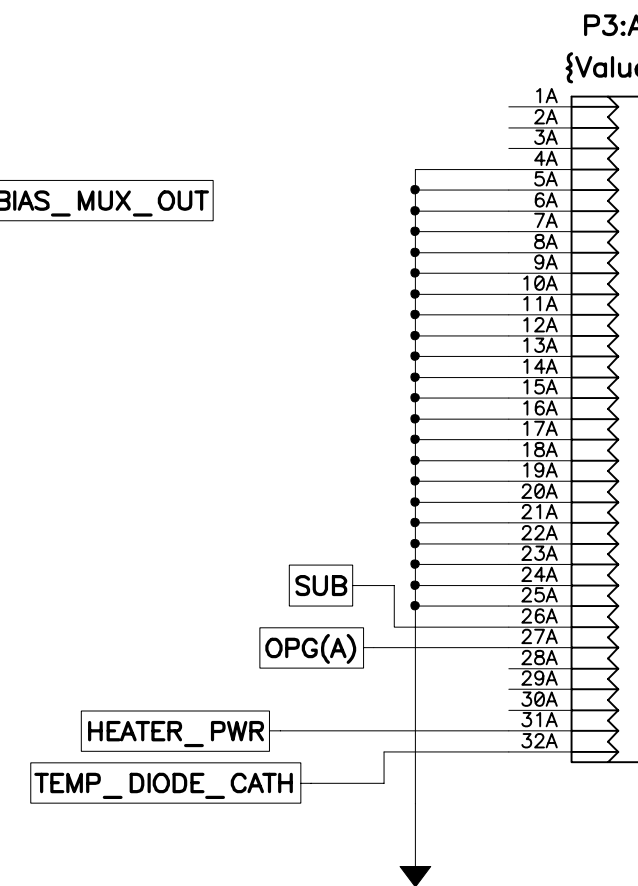
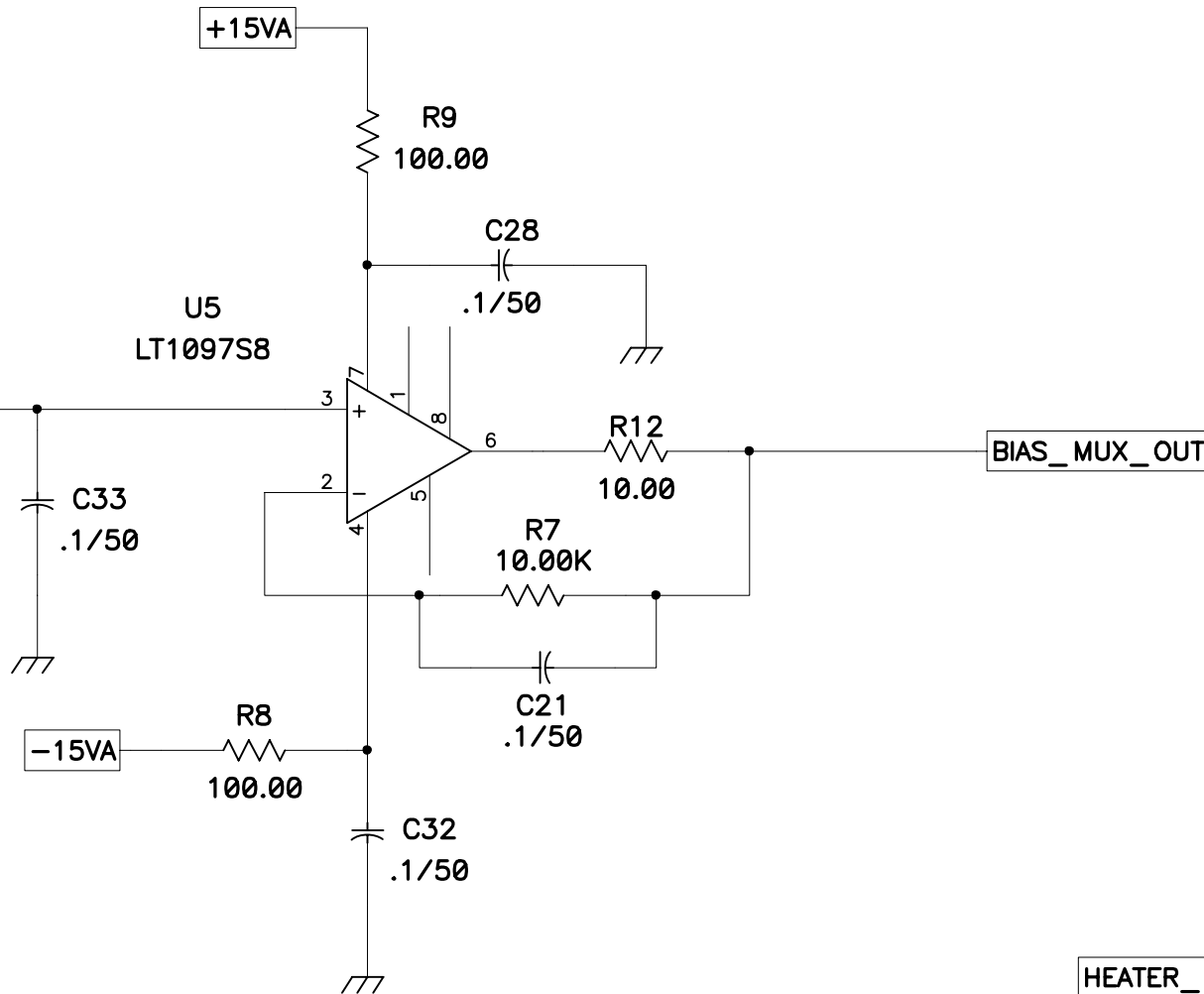
UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	
61-PIN CABLE INTERCONNECT	
DWG. NO.	EL-3194
DES'N BY: Chris Wright	ORIGIN DATE: APRIL 20, 1998
DRAWN BY:	MODIFY DATE:
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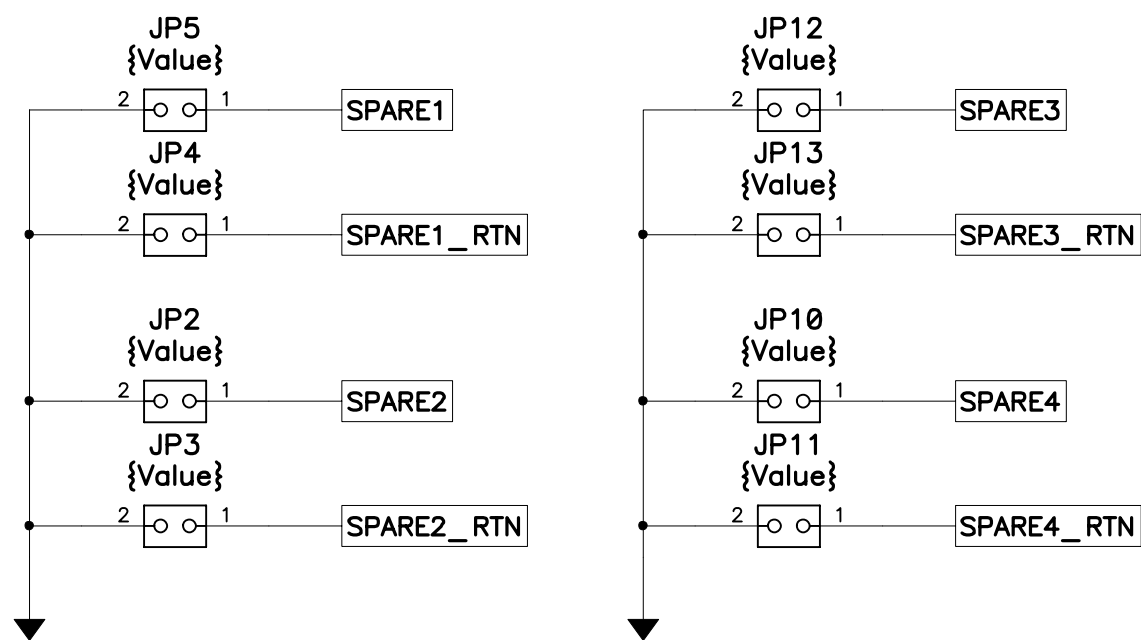
CCD'S SIGNALS' TEST CONNECTOR



CCD'S BIAS VOLTAGE MULTIPLEXER



OUTPUT CONNECTOR'S SPARE LINES' JUMPERS



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61-PIN CABLE INTERCONNECT	
DWG. NO.	EL-3194
DES'N BY: Chris Wright	ORIGIN DATE: APRIL 20, 1998
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CCD	SYSTEM CONFIGURATION	BIAS VOLTAGES			CLOCKS			
		P6 CONNECTED	JUMPER	JUMPERED PINS	P5 CONNECTED	JUMPER	JUMPERED PINS	
MITLL	SINGLE AMPLIFER READOUT	NO	JP14	1, 2	NO	JP17	2, 3	
			JP15	2, 3		JP20	1, 2	
			JP9	1, 2		JP19	1, 2	
			JP16	2, 3		JP18	1, 2	
			JP7	1, 2				
			JP21	2, 3				
			JP6	1, 2				
		JP8	1, 2					
	DUAL AMPLIFER READOUT	YES		JP14	1, 2	NO	JP17	2, 3
				JP15	1, 2		JP20	1, 2
				JP9	1, 2		JP19	1, 2
				JP16	1, 2		JP18	1, 2
				JP7	1, 2			
				JP21	1, 2			
				JP6	1, 2			
		JP8	1, 2					
SINGLE AMPLIFER READOUT W/ FRAME TRANSFER	NO		JP14	1, 2	YES REQUIRES SPECIAL CABLE (SEE EL-3176-2W)	JP17	2, 3	
			JP15	2, 3		JP20	2, 3	
			JP9	1, 2		JP19	2, 3	
			JP16	2, 3		JP18	2, 3	
			JP7	1, 2				
			JP21	2, 3				
			JP6	1, 2				
	JP8	1, 2						
DUAL AMPLIFER READOUT W/ FRAME TRANSFER	YES		JP14	1, 2	YES REQUIRES 2ND CLOCK BOARD	JP17	2, 3	
			JP15	1, 2		JP20	2, 3	
			JP9	1, 2		JP19	2, 3	
			JP16	1, 2		JP18	2, 3	
			JP7	1, 2				
			JP21	1, 2				
			JP6	1, 2				
	JP8	1, 2						
LICK/ORBIT	SINGLE AMPLIFER READOUT	NO	JP14	1, 2	YES REQUIRES SPECIAL CABLE (SEE EL-3176-2W)	JP17	1, 2	
			JP15	2, 3		JP20	1, 2	
			JP9	1, 2		JP19	1, 2	
			JP16	2, 3		JP18	1, 2	
			JP7	1, 2				
			JP21	2, 3				
			JP6	1, 2				
		JP8	2,3					
	DUAL AMPLIFER READOUT	YES		JP14	1, 2	YES REQUIRES 2ND CLOCK BOARD	JP17	1, 2
				JP15	1, 2		JP20	1, 2
				JP9	1, 2		JP19	1, 2
				JP16	1, 2		JP18	1, 2
				JP7	1, 2			
				JP21	1, 2			
JP6				1, 2				
	JP8	2, 3						

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61-PIN CABLE INTERCONNECT	
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