CLOCK #1

37 PIN CONNECTOR

CLOCK GEN BOARD 1 AT: VME SLOT=14 DAC ADDR=8 SWITCH ADDR=2

PIN	NAME	CCD SIGNAL	CCD NUMBER	CODE	PIN	NAME
1	CLK0	PARALLEL 1	1	–	20	+12V
2	CLK1	PARALLEL 2	1	–	21	–12V
3	CLK2	PARALLEL 3	1	–	22	GND
4	CLK3	SUMMING WELL (A)	1	–	23	GND
5	CLK4	SERIAL PHASE #1 (A)	1	–	24	GND
6	CLK5	SERIAL PHASE #2 (A)	1	–	25	GND
7	CLK6	SERIAL PHASE #3	1	–	26	GND
8	CLK7	SERIAL PHASE #2 (B)	1	–	27	GND
9	CLK8	SERIAL PHASE #1 (B)	1	–	28	GND
10	CLK9	SUMMING WELL (B)	1	–	29	GND
11	CLK10	RESET GATE (A)	1	–	30	GND
12	CLK11	RESET GATE (B)	1	–	31	GND
13	CLK12	PARALLEL 1	2	–	32	GND
14	CLK13	PARALLEL 2	2	–		
15	CLK14	PARALLEL 3	2	–		
16	CLK15	SUMMING WELL (A)	2	–		
17	CLK16	SERIAL PHASE #1 (A)	2	–		
18	CLK17	SERIAL PHASE #2 (A)	2	–		
19	CLK18	SERIAL PHASE #3	2	–		
33	CLK19	SERIAL PHASE #2 (B)	2	–		
34	CLK20	SERIAL PHASE #1 (B)	2	–		
35	CLK21	SUMMING WELL (B)	2	–		
36	CLK22	RESET GATE (A)	2	–		
37	CLK23	RESET GATE (R)	2	–		

CLOCK #2

37 PIN CONNECTOR

CLOCK GEN BOARD 2 AT: VME SLOT=13 DAC ADDR=9 SWITCH ADDR=2

PIN	NAME	CCD SIGNAL	CCD NUMBER	CODE	PIN	NAME
1	CLK0	PARALLEL 1	3	–	20	+12V
2	CLK1	PARALLEL 2	3	–	21	–12V
3	CLK2	PARALLEL 3	3	–	22	GND
4	CLK3	SUMMING WELL (A)	3	–	23	GND
5	CLK4	SERIAL PHASE #1 (A)	3	–	24	GND
6	CLK5	SERIAL PHASE #2 (A)	3	–	25	GND
7	CLK6	SERIAL PHASE #3	3	–	26	GND
8	CLK7	SERIAL PHASE #2 (B)	3	–	27	GND
9	CLK8	SERIAL PHASE #1 (B)	3	–	28	GND
10	CLK9	SUMMING WELL (B)	3	–	29	GND
11	CLK10	RESET GATE (A)	3	–	30	GND
12	CLK11	RESET GATE (B)	3	–	31	GND
13	CLK12	PARALLEL 1	4	–	32	GND
14	CLK13	PARALLEL 2	4	–		
15	CLK14	PARALLEL 3	4	–		
16	CLK15	SUMMING WELL (A)	4	–		
17	CLK16	SERIAL PHASE #1 (A)	4	–		
18	CLK17	SERIAL PHASE #2 (A)	4	–		
19	CLK18	SERIAL PHASE #3	4	–		
33	CLK19	SERIAL PHASE #2 (B)	4	–		
34	CLK20	SERIAL PHASE #1 (B)	4	–		
35	CLK21	SUMMING WELL (B)	4	–		
36	CLK22	RESET GATE (A)	4	–		
37	CLK23	RESET GATE (B)	4	–		

REVISION

10–20–97 Changed clock signal names "–L", "–R", "–L/R" to "–A", "–B", "–A/B" to eliminate left/right "view" ambiguity; added horiz. & vertical sync clocks

11–08–99 Updated VME slot numbers and dac addresses for reflect actual controller

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

PIN ASSIGNMENTS
CLOCK BOARD OUTPUT CONNECTORS
SDSU2 CCD CONTROLLER
DEIMOS SPECTROGRAPH

DES'N BY: B. Alcott | ORIGIN DATE: 04–27–97

DRAWN BY: | MODIFY DATE: 11–08–99

PATH: DEIMOS\SDSUCCD2\CLOCKCON | REV. A

DWG. NO. EL–3164–1D

NUM. 1 OF 3

CLOCK #3

37 PIN CONNECTOR

CLOCK GEN BOARD 3 AT: VME SLOT=3 DAC ADDR=10 SWITCH ADDR=2

PIN	NAME	CCD SIGNAL	CCD NUMBER	CODE	PIN	NAME
1	CLK0	PARALLEL 1	5	–	20	+12V
2	CLK1	PARALLEL 2	5	–	21	–12v
3	CLK2	PARALLEL 3	5	–	22	GND
4	CLK3	SUMMING WELL (A)	5	–	23	GND
5	CLK4	SERIAL PHASE #1 (A)	5	–	24	GND
6	CLK5	SERIAL PHASE #2 (A)	5	–	25	GND
7	CLK6	SERIAL PHASE #3	5	–	26	GND
8	CLK7	SERIAL PHASE #2 (B)	5	–	27	GND
9	CLK8	SERIAL PHASE #1 (B)	5	–	28	GND
10	CLK9	SUMMING WELL (B)	5	–	29	GND
11	CLK10	RESET GATE (A)	5	–	30	GND
12	CLK11	RESET GATE (A)	5	–	31	GND
13	CLK12	PARALLEL 1	6	–	32	GND
14	CLK13	PARALLEL 2	6	–		
15	CLK14	PARALLEL 3	6	–		
16	CLK15	SUMMING WELL (A)	6	–		
17	CLK16	SERIAL PHASE #1 (A)	6	–		
18	CLK17	SERIAL PHASE #2 (A)	6	–		
19	CLK18	SERIAL PHASE #3	6	–		
33	CLK19	SERIAL PHASE #2 (B)	6	–		
34	CLK20	SERIAL PHASE #1 (B)	6	–		
35	CLK21	SUMMING WELL (B)	6	–		
36	CLK22	RESET GATE (A)	6	–		
37	CLK23	RESET GATE (B)	6	–		

CLOCK #4

37 PIN CONNECTOR

CLOCK GEN BOARD 4 AT: VME SLOT=2 DAC ADDR=11 SWITCH ADDR=2

PIN	NAME	CCD SIGNAL	CCD NUMBER	CODE	PIN	NAME
1	CLK0	PARALLEL 1	7	–	20	+12V
2	CLK1	PARALLEL 2	7	–	21	–12v
3	CLK2	PARALLEL 3	7	–	22	GND
4	CLK3	SUMMING WELL (A)	7	–	23	GND
5	CLK4	SERIAL PHASE #1 (A)	7	–	24	GND
6	CLK5	SERIAL PHASE #2 (A)	7	–	25	GND
7	CLK6	SERIAL PHASE #3	7	–	26	GND
8	CLK7	SERIAL PHASE #2 (B)	7	–	27	GND
9	CLK8	SERIAL PHASE #1 (B)	7	–	28	GND
10	CLK9	SUMMING WELL (B)	7	–	29	GND
11	CLK10	RESET GATE (A)	7	–	30	GND
12	CLK11	RESET GATE (A)	7	–	31	GND
13	CLK12	PARALLEL 1	8	–	32	GND
14	CLK13	PARALLEL 2	8	–		
15	CLK14	PARALLEL 3	8	–		
16	CLK15	SUMMING WELL (A)	8	–		
17	CLK16	SERIAL PHASE #1 (A)	8	–		
18	CLK17	SERIAL PHASE #2 (A)	8	–		
19	CLK18	SERIAL PHASE #3	8	–		
33	CLK19	SERIAL PHASE #2 (B)	8	–		
34	CLK20	SERIAL PHASE #1 (B)	8	–		
35	CLK21	SUMMING WELL (B)	8	–		
36	CLK22	RESET GATE (A)	8	–		
37	CLK23	RESET GATE (B)	8	–		

REVISION

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

PIN ASSIGNMENTS
CLOCK BOARD OUTPUT CONNECTORS
SDSU2 CCD CONTROLLER
DEIMOS SPECTROGRAPH

DES'N BY: B. Alcott
ORIGIN DATE: 04–27–97
DRAWN BY:
MODIFY DATE:
PATH: DEIMOS\SDSUCCD2\CLOCKCON
REV. A

DWG. NO.
NUM. 2 OF 3

EL–3164–1D

CLOCK #5
37 PIN CONNECTOR

CLOCK GEN BOARD 5 AT: VME SLOT=15 DAC ADDR=12 SWITCH ADDR=4

PIN	NAME	CCD SIGNAL	CCD NUMBER	CODE	PIN	NAME
1	CLK0	PARALLEL 1 (BOTTOM)	1	–	20	+12V
2	CLK1	PARALLEL 2 (BOTTOM)	1	–	21	–12V
3	CLK2	PARALLEL 3 (BOTTOM)	1	–	22	GND
4	CLK3	PARALLEL 1 (BOTTOM)	2	–	23	GND
5	CLK4	PARALLEL 2 (BOTTOM)	2	–	24	GND
6	CLK5	PARALLEL 3 (BOTTOM)	2	–	25	GND
7	CLK6	PARALLEL 1 (BOTTOM)	3	–	26	GND
8	CLK7	PARALLEL 2 (BOTTOM)	3	–	27	GND
9	CLK8	PARALLEL 3 (BOTTOM)	3	–	28	GND
10	CLK9	PARALLEL 1 (BOTTOM)	4	–	29	GND
11	CLK10	PARALLEL 2 (BOTTOM)	4	–	30	GND
12	CLK11	PARALLEL 3 (BOTTOM)	4	–	31	GND
13	CLK12	PARALLEL 1 (BOTTOM)	5*	–	32	GND
14	CLK13	PARALLEL 2 (BOTTOM)	5*	–		
15	CLK14	PARALLEL 3 (BOTTOM)	5*	–		
16	CLK15	PARALLEL 1 (BOTTOM)	6*	–		
17	CLK16	PARALLEL 2 (BOTTOM)	6*	–		
18	CLK17	PARALLEL 3 (BOTTOM)	6*	–		
19	CLK18	PARALLEL 1 (BOTTOM)	7*	–		
33	CLK19	PARALLEL 2 (BOTTOM)	7*	–		
34	CLK20	PARALLEL 3 (BOTTOM)	7*	–		
35	CLK21	PARALLEL 1 (BOTTOM)	8*	–		
36	CLK22	HORIZONTAL SYNC	–	–		
37	CLK23	VERTICAL SYNC	–	–		

* DIAGNOSTIC PURPOSES ONLY.

MIT/LINCOLN LABS CCDS OR SITE CCDS WITH FRAME TRANSFER

CLOCK #5
37 PIN CONNECTOR

CLOCK GEN BOARD 5 AT: VME SLOT=15 DAC ADDR=12 SWITCH ADDR=4

PIN	NAME	CCD SIGNAL	CCD NUMBER	CODE	PIN	NAME
1	CLK0	TRANSFER GATE	1	–	20	+12V
2	CLK1	TRANSFER GATE	2	–	21	–12V
3	CLK2	TRANSFER GATE	3	–	22	GND
4	CLK3	TRANSFER GATE	4	–	23	GND
5	CLK4	TRANSFER GATE	5	–	24	GND
6	CLK5	TRANSFER GATE	6	–	25	GND
7	CLK6	TRANSFER GATE	7	–	26	GND
8	CLK7	TRANSFER GATE	8	–	27	GND
9	CLK8	–	–	–	28	GND
10	CLK9	–	–	–	29	GND
11	CLK10	–	–	–	30	GND
12	CLK11	–	–	–	31	GND
13	CLK12	–	–	–	32	GND
14	CLK13	–	–	–		
15	CLK14	–	–	–		
16	CLK15	–	–	–		
17	CLK16	–	–	–		
18	CLK17	–	–	–		
19	CLK18	–	–	–		
33	CLK19	–	–	–		
34	CLK20	–	–	–		
35	CLK21	–	–	–		
36	CLK22	HORIZONTAL SYNC*	–	–		
37	CLK23	VERTICAL SYNC*	–	–		

* DIAGNOSTIC PURPOSES ONLY.

LICK ORBIT CCDS

REVISION

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

PIN ASSIGNMENTS
CLOCK BOARD OUTPUT CONNECTORS
SDSU2 CCD CONTROLLER
DEIMOS SPECTROGRAPH

DES'N BY: B. Alcott
ORIGIN DATE: 04–27–97
DRAWN BY:
MODIFY DATE: 11–09–99
PATH: DEIMOS\SDSUCCD2\CLOCKCON
REV. A

DWG. NO. EL–3164–1D
NUM. 3 OF 3