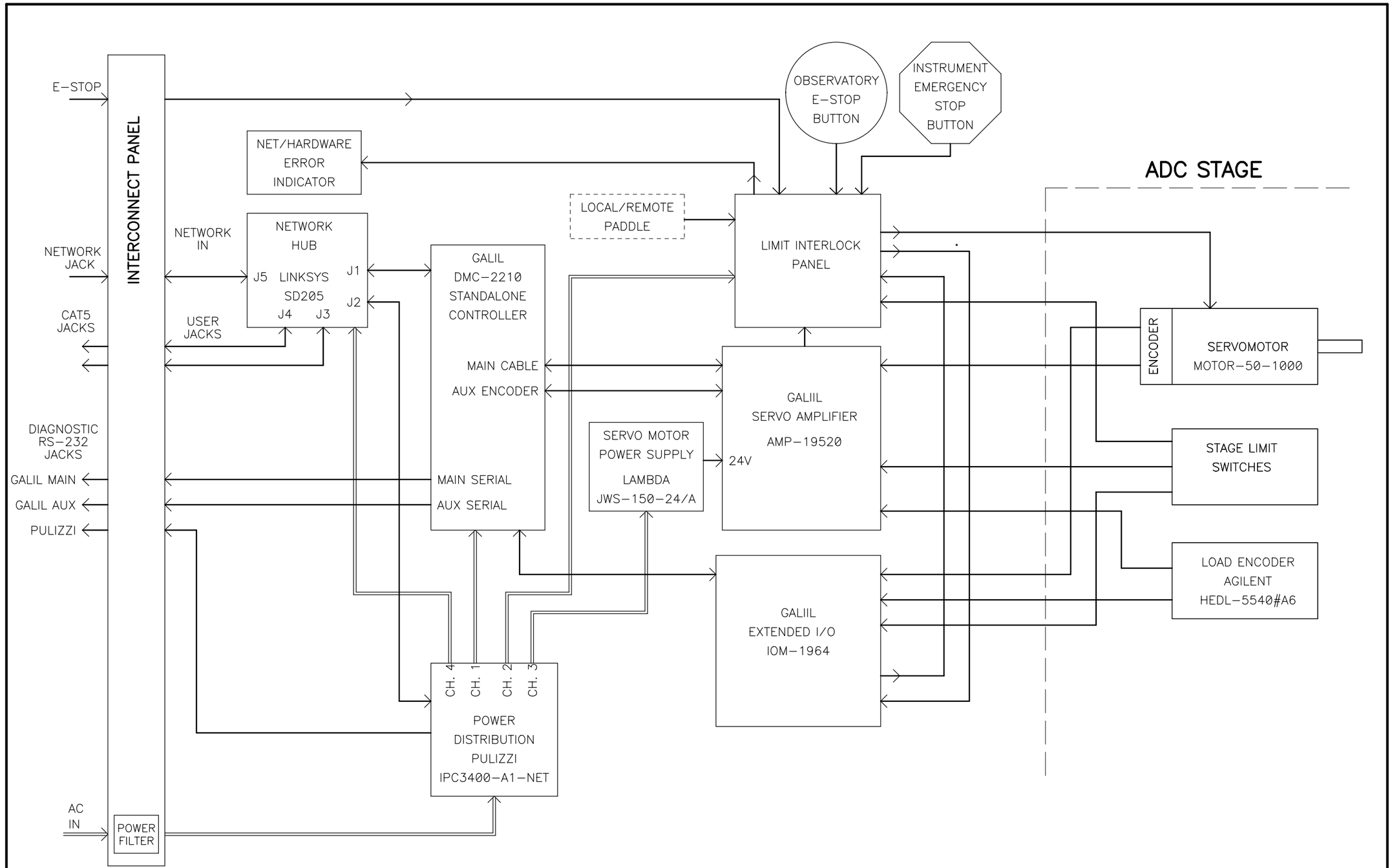
ADC DRAWINGS

EL–	PCAD FILE	DESCRIPTION
3600	LRIS_ADC\ 3600	This sheeet
3601	LRIS_ADC\ ADC_block	Overall block diagram
3602	LRIS_ADC\ –	–
3603	LRIS_ADC\ ADC_relay_driver	DC relay driver board
3604	LRIS_ADC\ ADC_LED_driver	LED driver board
3605	LRIS_ADC\ ADC_limit_sensors	Limit sensor boards
3606	LRIS_ADC\ ADC_temperature	Temperature monitoring
3607	LRIS_ADC\ ADC_defining_point_wiring	Defining point solenoid wiring
3608	LRIS_ADC\ ADC_in_out	Extended I/O bit assignments
3609	LRIS_ADC\ –	–
3610	LRIS_ADC\ ADC_stage	Prism stage wiring
3611	LRIS_ADC\ ADC_stage_cables	Prism stage cable wiring
3612	LRIS_ADC\ ADC_interlock	Limit/Power interlock wiring
3613	LRIS_ADC\ ADC_interlock_cables	Interlock cable wiring
3614	LRIS_ADC\ ADC_misc_wiring	Wiring inside the cabinet not covered elsewhere
3615	LRIS_ADC\ –	–
1356	GENERAL\EL1356\4ch_temp_sensor	4 Input temperature sensor board for Galil IOM–19520/40
–	– –	–
–	– –	–

3600.SCH

SHEET 1 OF 1

MODIFIED: 02–08–05



http://loel.ucolick.org/manual/ADC/schematics/ADC_ block_ SH1.sch.pdf

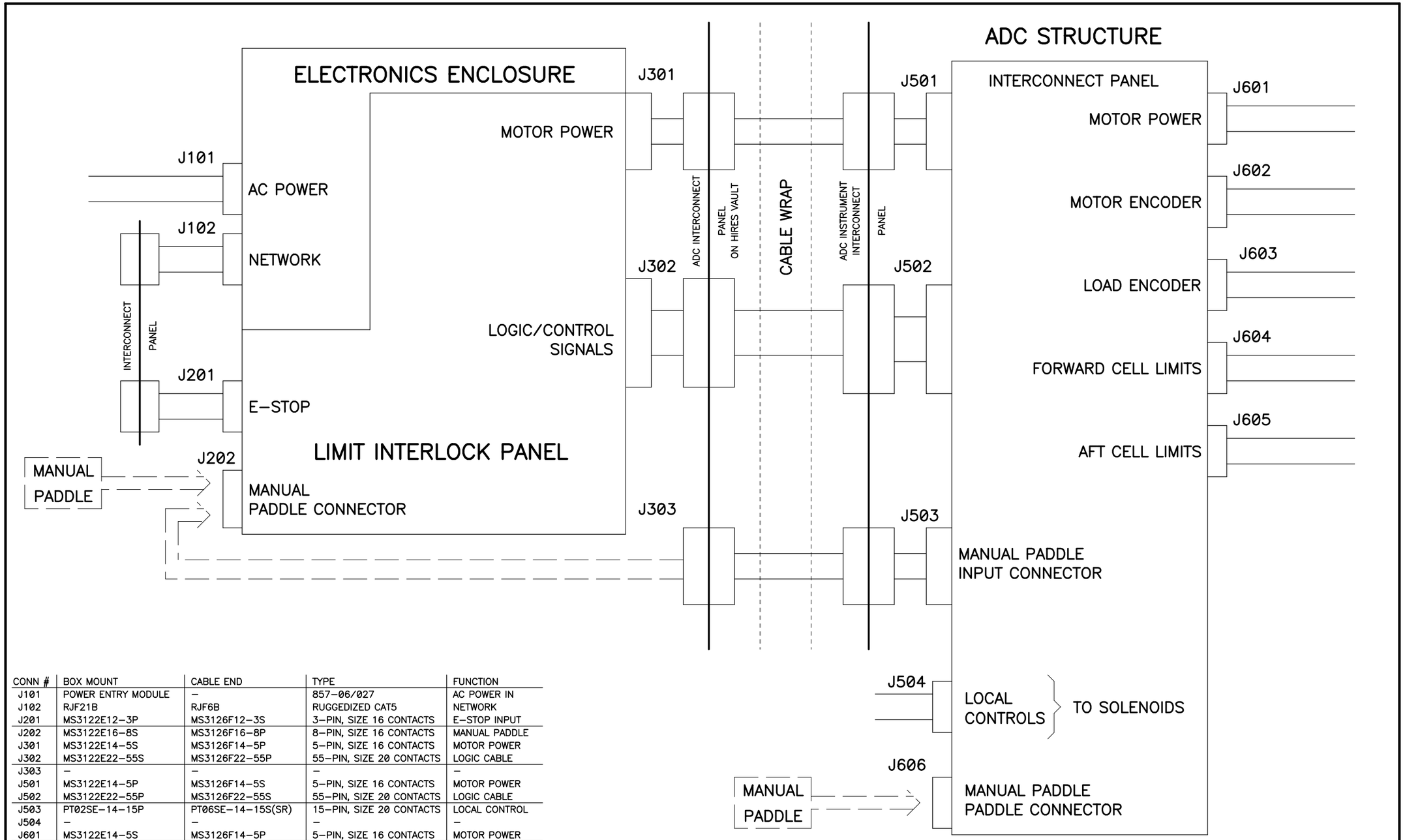
REVISION

02-23-04	MOVED PREVIOUS 1ST SHEET OF INTERLOCK DIAGRAM TO 2ND SHEET OF THIS SCHEMATIC
02-24-04	RE-LAYED OUT SHEET 1 FOR BETTER CLARITY
03-05-04	CORRECTED GALIL AMPLIFIER PART NUMBER FROM AMP-1910 TO AMP-19520
03-15-04	REMOVED EQUIPMENT CONCERNED WITH COOLING AND TERMINAL SERVER PENDING USE OF HIRES ELECTRONICS VAULT
04-02-04	ADDED J202 PART NUMBERS ON SHEET 2
04-14-04	ADDED AUXILIARY ENCODER CABLE TO THIS SHEET
05-05-04	CHANGED J503 LABEL TO LOCAL CONTROLS AND ADDED J607 FOR NEW PADDLE KECK WANTS ADDED
06-09-04	RELABELED LOCAL/REMOTE SWITCH, ADD POWER STRIP, AND ADDED CONNECTION BETWEEN STAGE LIMITS AND INTERLOCK BLOCK
01-21-05	RELABELED NETWORK HUB PER PURCHASED UNIT AND CONNECTED IT TO THE PULIZZI POWER CONTROLLER

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

KECK ADC
BLOCK DIAGRAM

DES'N BY: B. Alcott	ORIGIN DATE: 08-20-03	DWG. NO.	NUM. 1 OF 3
Last SN	MODIFY DATE: 01-21-05	EL-3601	REV. B
PRINT TIME: 11:23:59	PRINT DATE: Fri Jan 21, 2005		
PATH: ADC/		ADC_ block_ Rev_ B.sch	



CONN #	BOX MOUNT	CABLE END	TYPE	FUNCTION
J101	POWER ENTRY MODULE	–	857–06/027	AC POWER IN
J102	RJF21B	RJF6B	RUGGEDIZED CAT5	NETWORK
J201	MS3122E12–3P	MS3126F12–3S	3–PIN, SIZE 16 CONTACTS	E–STOP INPUT
J202	MS3122E16–8S	MS3126F16–8P	8–PIN, SIZE 16 CONTACTS	MANUAL PADDLE
J301	MS3122E14–5S	MS3126F14–5P	5–PIN, SIZE 16 CONTACTS	MOTOR POWER
J302	MS3122E22–55S	MS3126F22–55P	55–PIN, SIZE 20 CONTACTS	LOGIC CABLE
J303	–	–	–	–
J501	MS3122E14–5P	MS3126F14–5S	5–PIN, SIZE 16 CONTACTS	MOTOR POWER
J502	MS3122E22–55P	MS3126F22–55S	55–PIN, SIZE 20 CONTACTS	LOGIC CABLE
J503	PT02SE–14–15P	PT06SE–14–15S(SR)	15–PIN, SIZE 20 CONTACTS	LOCAL CONTROL
J504	–	–	–	–
J601	MS3122E14–5S	MS3126F14–5P	5–PIN, SIZE 16 CONTACTS	MOTOR POWER
J602	MS3122E12–10S	MS3126F12–10P	10–PIN, SIZE 20 CONTACTS	MOTOR ENCODER
J603	MS3122E12–10P	MS3126F12–10S	10–PIN, SIZE 20 CONTACTS	LOAD ENCODER
J604	MS3122E18–11S	MS3126F18–11P	11–PIN, SIZE 16 CONTACTS	FWD CELL LIM
J605	MS3122E18–11P	MS3126F18–11S	11–PIN, SIZE 16 CONTACTS	AFT CELL LIM
J606	MS3122E16–8S	MS3126F16–8P	8–PIN, SIZE 16 CONTACTS	MANUAL PADDLE
J701	DB25P	DB25S	25–PIN	IOM SIGNALS
J702	HI DENSITY DB15P	HI DENSITY DB15S	15–PIN	IOM SIGNALS

http://loel.ucolick.org/manual/ADC/schematics/ADC_block_SH_2.sch.pdf

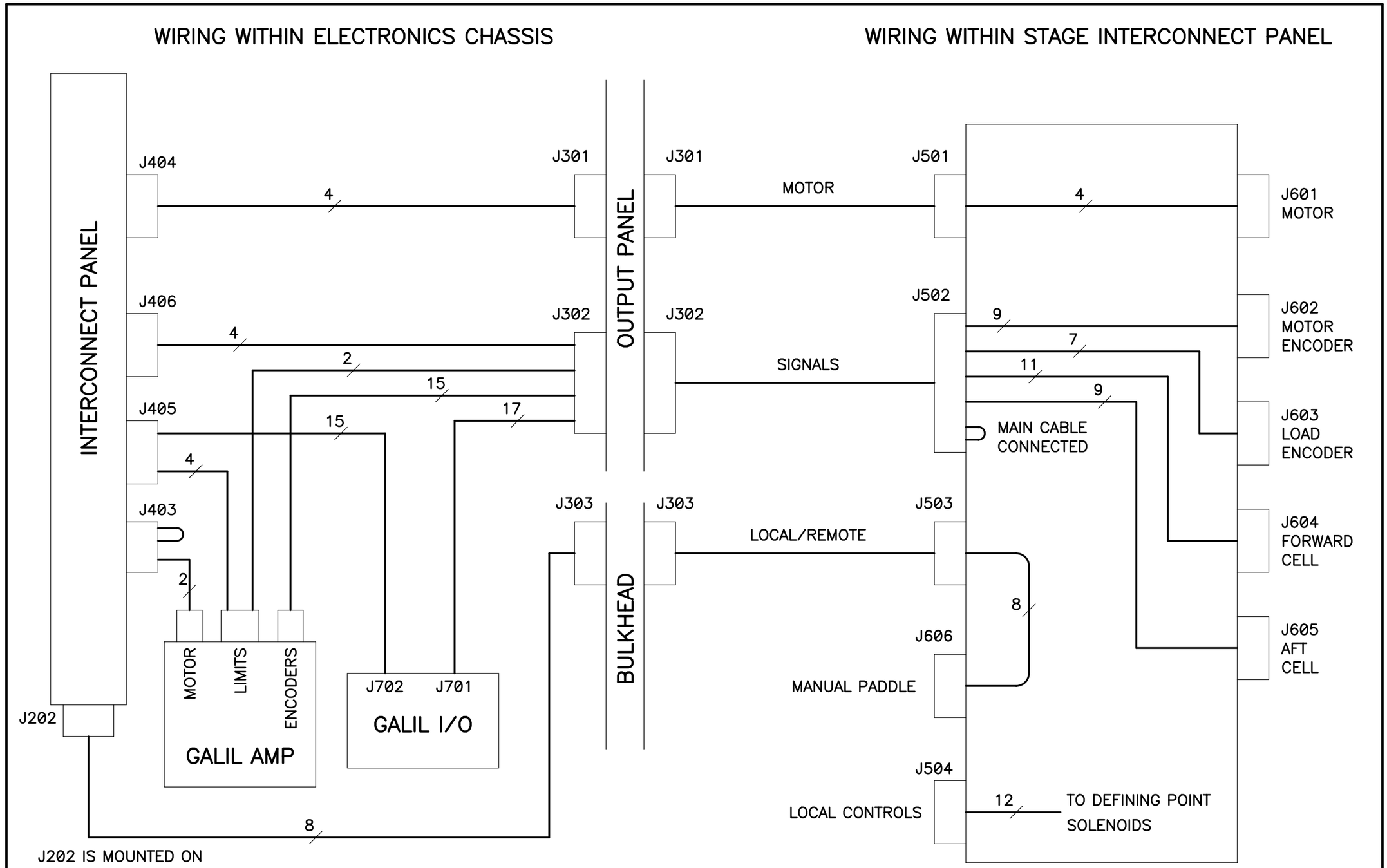
REVISION

04–20–04 CHANGED ALL CONNECTOR NUMBERS
05–05–04 CHANGED J503 LABEL TO LOCAL CONTROLS AND ADDED J607 FOR NEW PADDLE KECK WANTS ADDED
05–12–04 ADDED HIRES ENCLOSURE BULKHEAD CONNECTORS
05–14–04 UPDATED CONNECTOR PART NUMBER TABLE
05–21–04 ADDED INTERCONNECT PANELS PER KECK
05–25–04 CHANGED ALL MS3120 CONNECTORS TO MS3122 STYLE
06–09–04 RENAMED NULL PADDLE TO MANUAL PADDLE, ADDED THIRD CABLE BETWEEN ELECTRONICS AND STAGE FOR MANUAL PADDLE AND CHANGED J503 TO J504. MOVED J607 TO J606
11–24–04 UPDATED CONNECTOR PART NUMBER INFO

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

KECK ADC
BLOCK DIAGRAM

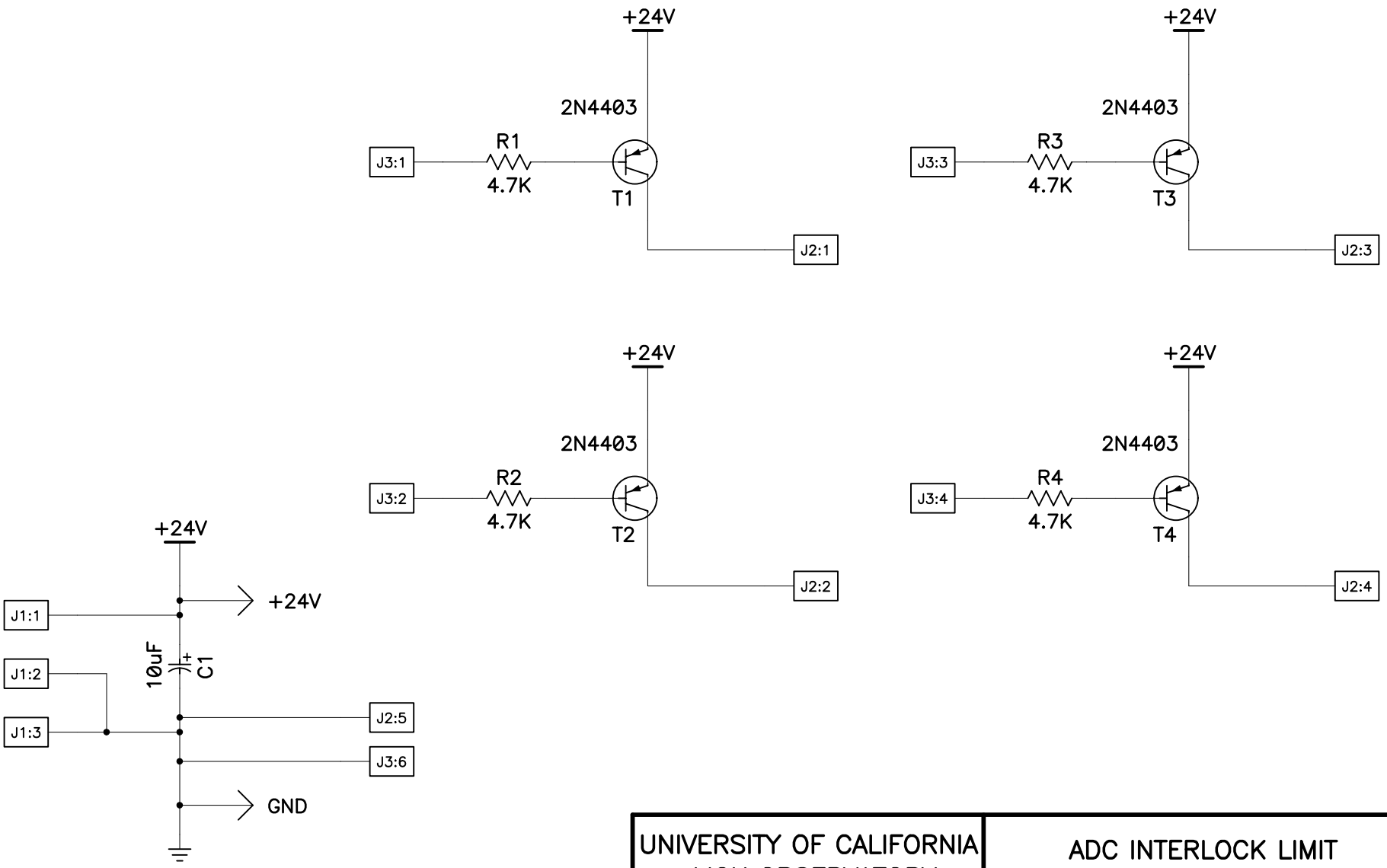
DES'N BY: B. Alcott	ORIGIN DATE: 08–20–03	DWG. NO.	NUM. 2 OF 3
Last SN	MODIFY DATE: 11–24–04	EL–3601	REV. B
PRINT TIME: 11:44:02	PRINT DATE: Wed Nov 24, 2004		
PATH: ADC/		ADC_block_Rev_B.sch	



REVISION

06-15-04 ADDED THIS SHEET
02-07-05 ADDED CONNECTOR NUMBERS J701 AND J702 TO GALIL I/O BLOCK

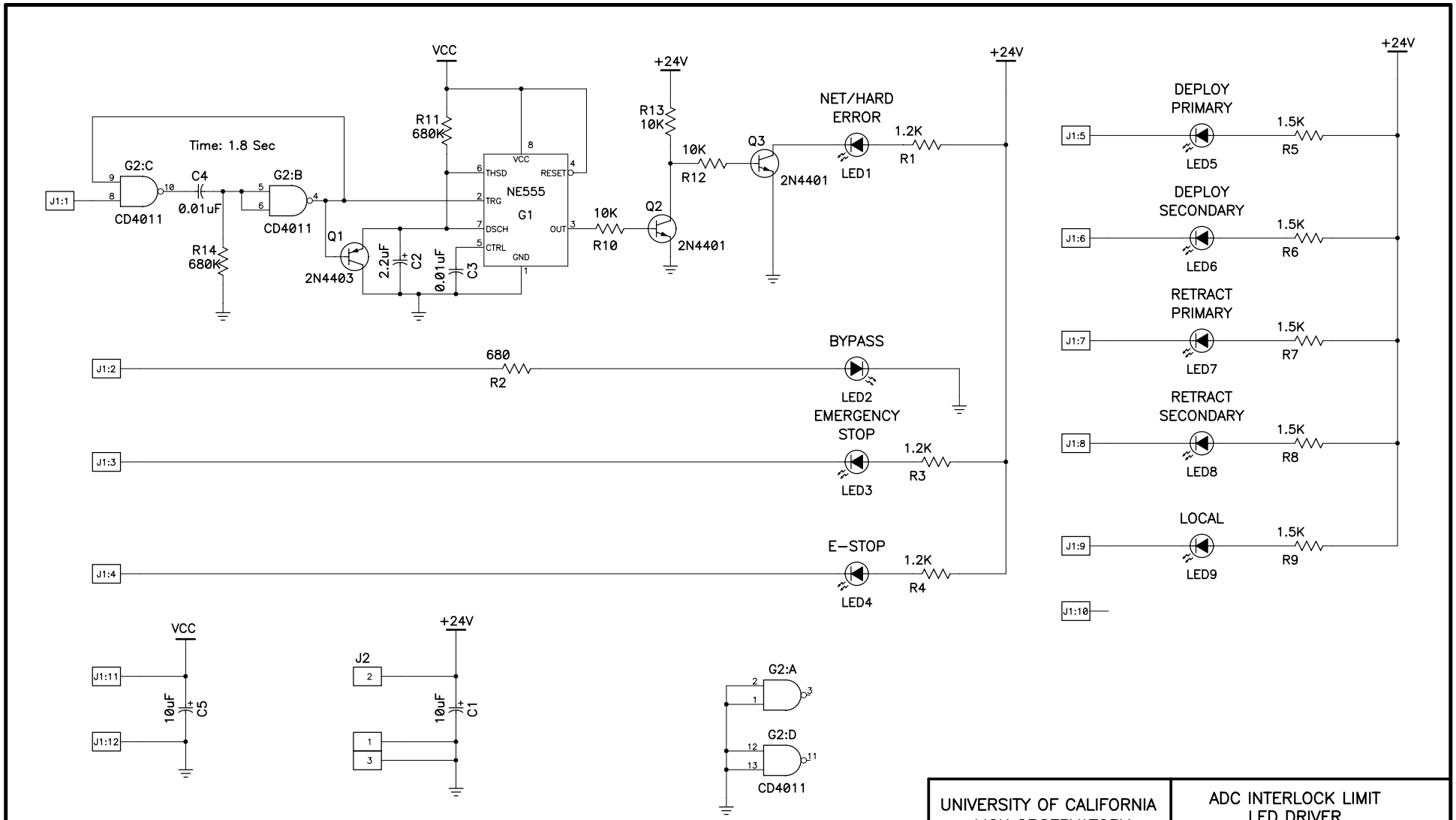
UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		KECK ADC BLOCK DIAGRAM	
DES'N BY: B. Alcott	ORIGIN DATE: 08-20-03	DWG. NO. EL-3601	NUM. 3 OF 3
Last SN	MODIFY DATE: 02-07-05		REV. B
PRINT TIME: 07:33:17	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC/		ADC_ block_ Rev_ B.sch	



REVISION

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	ADC INTERLOCK LIMIT RELAY DRIVER

DES'N BY: B. Alcott	ORIGIN DATE: 09-20-04	DWG. NO.	NUM. OF 1
Last SN	MODIFY DATE:	EL-3603	REV. A
PRINT TIME: 13:37:31	PRINT DATE: Tue Oct 12, 2004		
PATH: {Path}		relay_driver.sch	



REVISIONS

Rev. B: Added C4 and R14 to turn on LED when input is constant LOW
01-12-05 Rev. C: Replaced C4 and R14 with a One-shot Multivibrator
01-12-05 Rev. C: Replaced C4 and R14 with a One-shot Multivibrator
01-12-05 REV. D. REMOVED 15V REGULATOR - USING 5V NOW

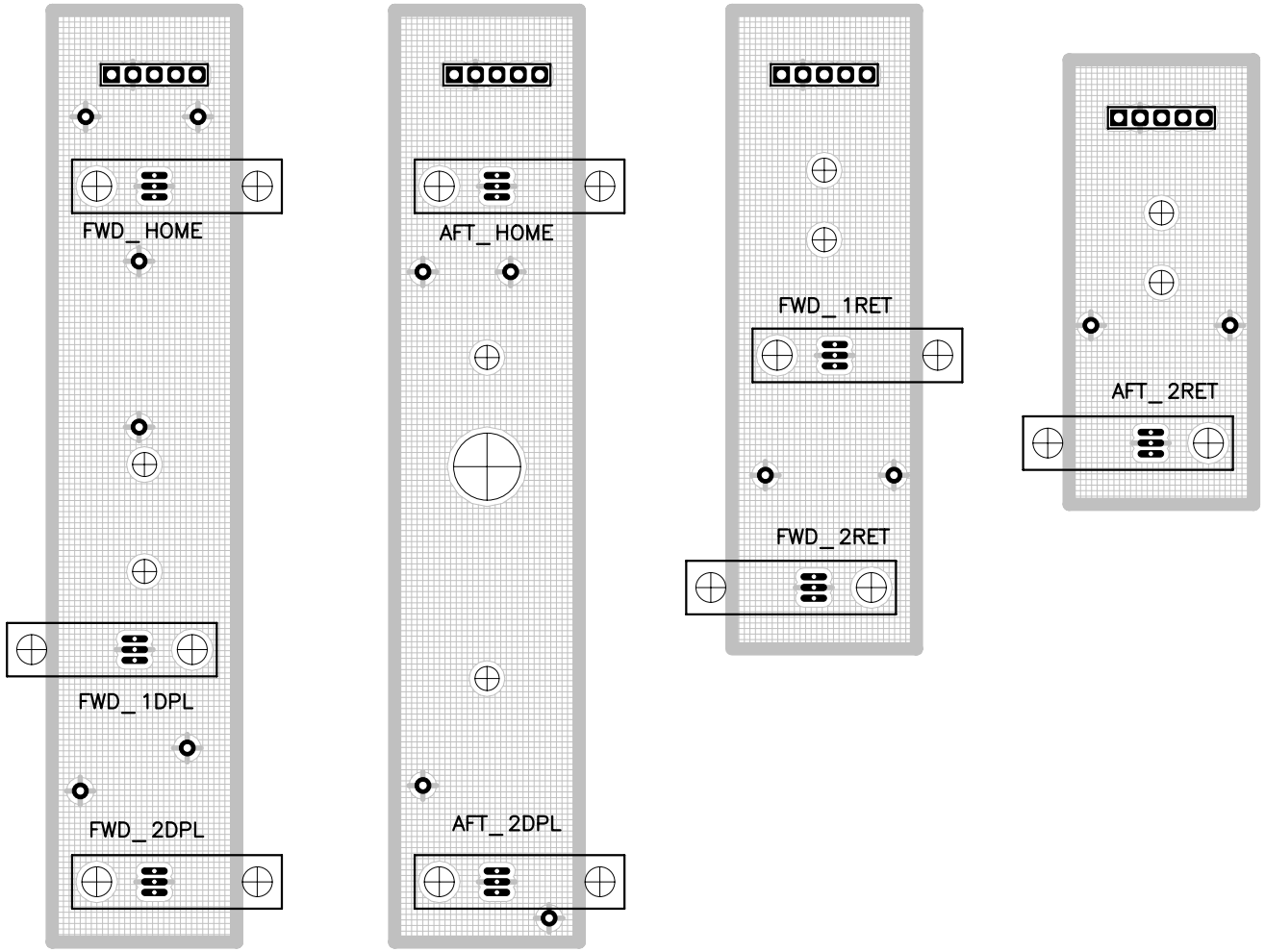
UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	ADC INTERLOCK LIMIT LED DRIVER

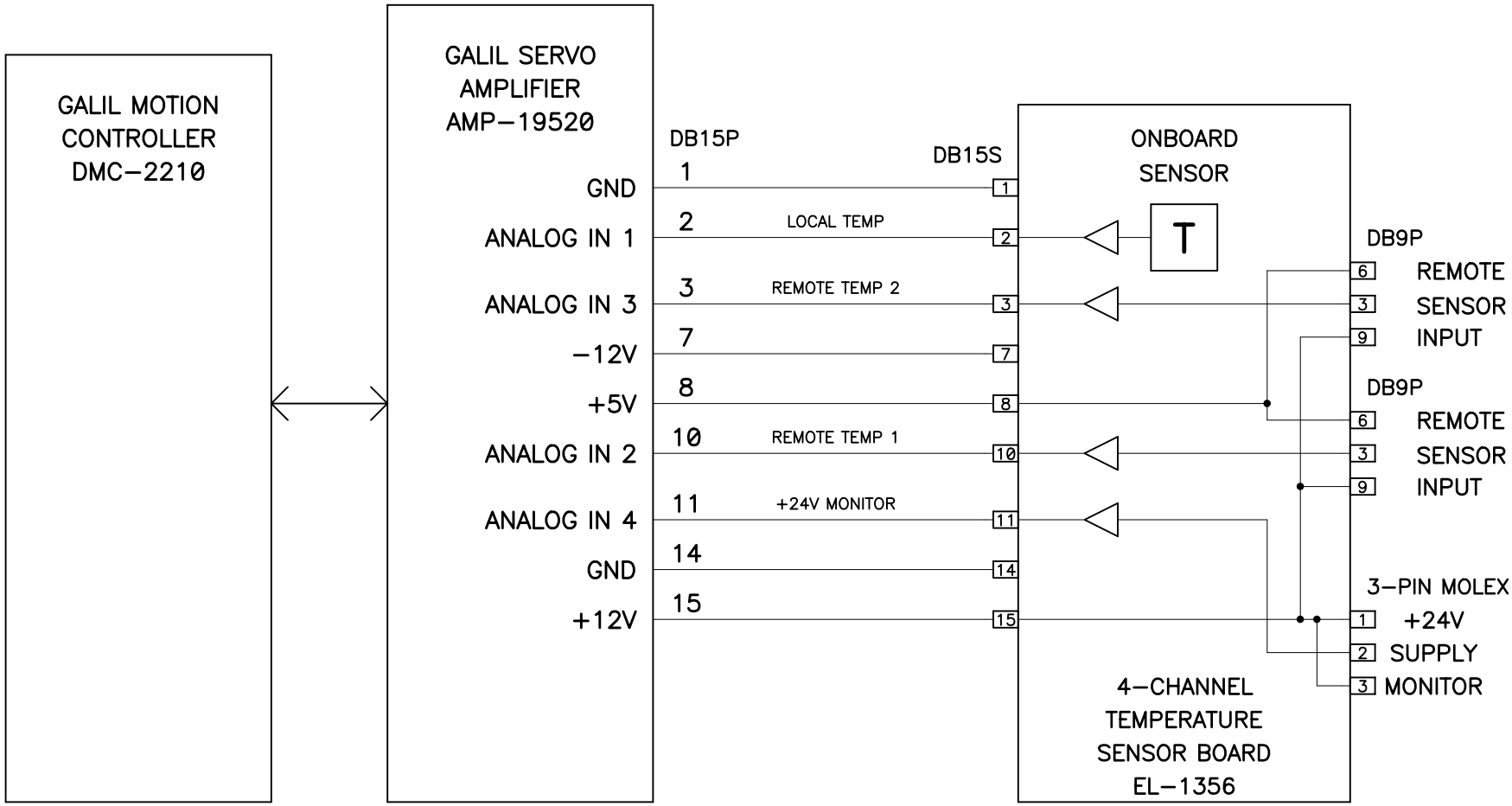
DES'N BY: B. Alcott	ORIGIN DATE: 01-07-05	DWG. NO. EL-3604	NUM. 1 OF 1
Last SN	MODIFY DATE: 01-12-05		REV. D
PRINT TIME: 15:16:03	PRINT DATE: Fri Feb 04, 2005		
PATH: /ADC/boards		ADC_LED_driver.sch	

NUM. 1 OF 1

ADC LED Driver

EL-3604

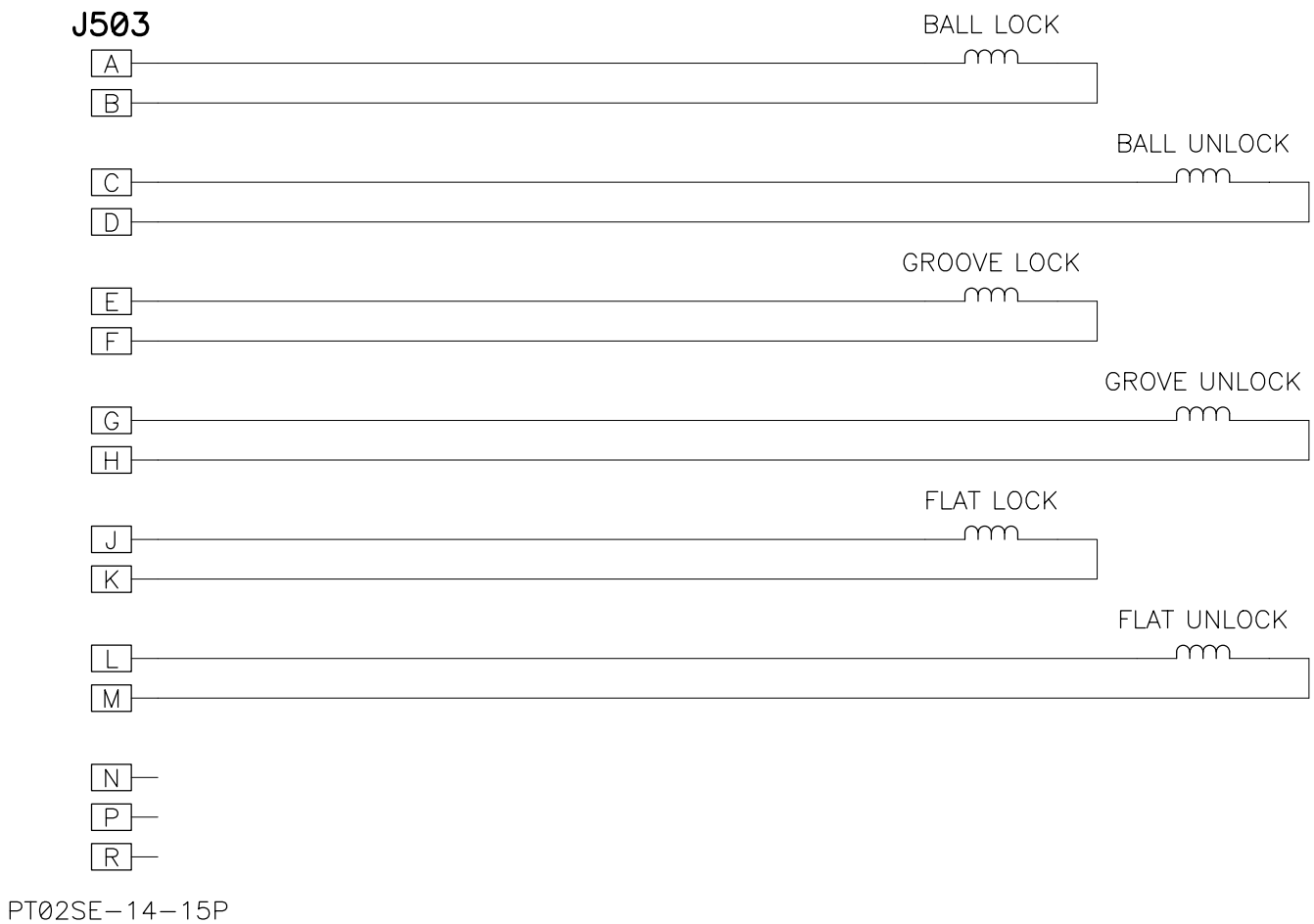

FWD_ HOME
FWD_ 1DPL
FWD_ 2DPL
AFT_ HOME
AFT_ 2DPL
FWD_ 1RET
FWD_ 2RET
AFT_ 2RET



http://loel.ucolick.org/manual/ADC/schematics/ADC_ temperature.sch.pdf

REVISION
04-12-04 CHANGED TO 4 INPUT TEMPERATURE BOARD 05-05-04 CHANGED +24V LABELS TO MONITOR

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	KECK ADC TEMPERATURE SENSOR WIRING
DES'N BY: B. Alcott	ORIGIN DATE: 03-29-04
Last SN	MODIFY DATE: 05-05-04
PRINT TIME: 08:03:11	PRINT DATE: Thu May 06, 2004
DWG. NO. EL-3606	NUM. OF 1
REV. A	
PATH: ADC	ADC_ temperature.sch



REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_defining_point_wiring.sch.pdf

03-05-04 ADDED CONNECTOR P/N AND CORRECTED REFERENCE DESIGNATION FROM P1 TO J204
04-21-04 CHANGED CONNECTOR NUMBER FROM J204 TO J503
05-05-04 REMOVED CABLE CONNECTED WIRING

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		KECK ADC DEFINING POINT WIRING	
DES'N BY: B. Alcott	ORIGIN DATE: 10-06-03	DWG. NO. EL-3607	NUM. 1 OF 1
Last SN	MODIFY DATE: 05-05-04		REV. A
PRINT TIME: 08:03:41	PRINT DATE: Thu May 06, 2004		
PATH: ADC		ADC_defining_point_wiring.sch	

NUM. 1 OF 1

KECK ADC DEFINING POINT WIRING

EL-3607

ADC EXTENDED I/O BITS 17 – 48*

	BIT	PIN	I/O	SIGNAL	FUNCTION	TO
BLOCK 2, BANK 0		94		I/OC17–24	+5V	–
		93		OUTC17–24	–	–
	17	92	O	–	–	–
	18	91	O	–	–	–
	19	90	O	–	–	–
	20	89	O	–	–	–
	21	88	O	–	–	–
	22	87	O	–	–	–
	23	86	O	–	–	–
	24	85	O	–	–	–
BLOCK 3, BANK 1		74		I/OC25–32	+5V	–
		73		OUTC25–32	–	–
	25	72	O	–	–	–
	26	71	O	–	–	–
	27	70	O	–	–	–
	28	69	O	–	–	–
	29	68	O	–	–	–
	30	67	O	–	–	–
	31	66	O	–	–	–
	32	65	O	–	–	–

	BIT	PIN	I/O	SIGNAL	FUNCTION	TO
BLOCK 4, BANK 2		64		I/OC33–40	+5V	–
		63		OUTC33–40	GND	–
	33	62	O	$\overline{\text{NET/HARD_ERR}}$	NETWORK/HARDWARE ERROR LED	J702–3
	34	61	O	–	–	–
	35	60	O	–	–	–
	36	59	O	–	–	–
	37	58	O	–	–	–
	38	57	O	–	–	–
	39	56	O	–	–	–
	40	55	O	–	–	–
BLOCK 5, BANK 3		54		I/OC41–48	+5V	–
		53		OUTC41–48	–	–
	41	52	I	–	–	–
	42	51	I	–	–	–
	43	50	I	–	–	–
	44	49	I	–	–	–
	45	48	I	–	–	–
	46	47	I	–	–	–
	47	46	I	–	–	–
	48	45	I	–	–	–

* SEE SHEET 3 FOR HIGH POWER OUTPUTS

$$N = n0 + 2*n1 + 4*n2 + 8*n3 + 16*n4 + 32*n5 + 64*n6 + 128*n7$$

$$N = 0 + 0 + 4 + 0 + 0 + 0 + 0 + 0$$

FOR ADC, CO=4

NOTES: 1) I/O BIT NUMBERS STARTING WITH A 'P' DENOTE POWER DRIVER ABILITY

2) AS PER GALIL APP. NOTE #1438, TO USE BANKS 0 AND 1 FOR INPUTS, THE IOM–1964 CONNECTION LABELED OUTCn MUST BE CONNECTED TO THE ISOLATED POWER SUPPLY GROUND.

B

REVISIONS

04–14–04 ADDED NETWORK/HARDWARE ERROR OUTPUT TO BIT 35 AND ADDED 'TO' COLUMN
04–26–04 UPDATED SHEET 2
05–05–04 DROPED UNUSED OUTPUTS ($\overline{\text{DROP AC}}$, AND $\overline{\text{FANS ON}}$) AND UPDATED SHEET 2
05–27–04 REMOVED EMERGENCY NULL PADDLE INPUTS AT BITS 62 AND 63 AND ADDED EMERGENCY NULL MODE INPUT AT BIT 68 (SHEET 2)
10–13–04 ADDED SHEET 3 AND MOVED POWER OUTPUT PIN ASSIGNMENTS TO PAGE 3 (NONE OF THE POWER OUTPUTS ARE BEING USED AT THIS TIME) ALSO ADDED I/O AND OUT COMMON PINS
01–21–05 MOVED NET/HARDWARE SIGNAL FROM BIT 17 (HI POWER OUTPUT) TO BIT 33
01–26–05 CORRECTED I/O LABELS FOR BITS 33–40 FROM "I" TO "O"
02–07–05 CORRECTED NET/HARDWARE SIGNAL CONNECTION FROM J405–3 TO J701–3 (J701 IS THE CONNECTOR ON THE I/O PANEL AND J405 IS ON THE INTERLOCK PANEL)

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	ADC EXTENDED I/O SIGNALS AND WIRING KECK ADC

DES'N BY: B. Alcott	ORIGIN DATE: 02–11–04	DWG. NO. EL–3608	NUM. 1 OF 3
Last SN	MODIFY DATE: 02–07–05		REV. A
PRINT TIME: 07:33:56	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC\		ADC_in_out.sch	

ADC EXTENDED I/O BITS 49 – 80

	BIT	PIN	I/O	SIGNAL	FUNCTION	TO
BLOCK 6, BANK 4		44		I/OC49–56	+5V*	–
		43		OUTC49–56	–	–
	49	42	I	2RET (FWD_RET_2ND)	FWD CELL RETRACT 2ND LIMIT	J702–6
	50	41	I	2DPL (FWD_DEP_2ND)	FWD CELL DEPLOY 2ND LIMIT	J702–7
	51	40	I	AFT_RET_2ND	AFT CELL RETRACT 2ND LIMIT	J701–10
	52	39	I	AFT_DEP_2ND	AFT CELL DEPLOY 2ND LIMIT	J701–11
	53	38	I	AFT_HOME	AFT CELL HOME FIDUCIAL	J701–12
	54	37	I	–	–	–
	55	36	I	–	–	–
	56	35	I	–	–	–
BLOCK 7, BANK 5		34		I/OC57–64	+5V*	–
		33		OUTC57–64	–	–
	57	32	I	$\overline{\text{MOTOR_CONN}}$	MOTOR CABLE CONNECTED	J702–8
	58	31	I	$\overline{\text{MOTOR_ENCD_CONN}}$	MOTOR ENCODER CABLE CONNECTED	J701–15
	59	30	I	$\overline{\text{LOAD_ENCD_CONN}}$	LOAD ENCODER CABLE CONNECTED	J701–16
	60	29	I	$\overline{\text{FWD_CELL_CONN}}$	FORWARD CELL LIMIT CABLE CONNECTED	J701–17
	61	28	I	$\overline{\text{AFT_CELL_CONN}}$	AFT CELL LIMIT CABLE CONNECTED	J701–18
	62	27	I	$\overline{\text{MAN_PADDLE_CONN}}$	LOW WHEN PADDLE IS CONNECTED	J702–9
	63	26	I	$\overline{\text{MAIN_CABLE_CONN}}$	MAIN LOGIC CABLE IS CONNECTED	J701–2
	64	25	I	–	–	–

	BIT	PIN	I/O	SIGNAL	FUNCTION	TO
BLOCK 8, BANK 6		24		I/OC65–72	+5V*	–
		23		OUTC65–72	–	–
	65	22	I	E–STOP	OBSERVATORY E–STOP INPUT SIGNAL	J702–11
	66	21	I	EMERGENCY_STOP	EMERGENCY STOP BUTTON PUSHED	J702–5
	67	20	I	LOCAL/REMOTE	INSTRUMENT CONTROL SWITCH INPUT	J702–12
	68	19	I	BYPASS_MODE	EMERGENCY NULL MODE IN EFFECT	J702–13
	69	18	I	–	–	–
	70	17	I	–	–	–
	71	16	I	–	–	–
	72	15	I	–	–	–
BLOCK 9, BANK 7		14		I/OC73–80	+5V*	–
		13		OUTC73–80	–	–
	73	12	I	–	–	–
	74	11	I	–	–	–
	75	10	I	–	–	–
	76	9	I	–	–	–
	77	8	I	–	–	–
	78	7	I	–	–	–
	79	6	I	–	–	–
	80	5	I	–	–	–
		4		+5V	+5V DC OUT FROM J1	–
		3		GND	GROUND PINS OF J1	J701–1, 7, 9, 13
		2		+5V	+5V DC OUT FROM J1	J701–8
		1		GND	GROUND PINS OF J1	J702–1, 4, 12, 20, 21

*+5V IS DAISY CHAINED FROM TERMINALS 2 AND 4.

NOTES: 1) I/O BIT NUMBERS STARTING WITH A 'P' DENOTE POWER DRIVER ABILITY

2) AS PER GALIL APP. NOTE #1438, TO USE BANKS 0 AND 1 FOR INPUTS, THE IOM–1964 CONNECTION LABELED OUTCn MUST BE CONNECTED TO THE ISOLATED POWER SUPPLY GROUND.

B

REVISIONS

03–05–04 ADDED $\overline{\text{FLOW OK}}$ AND $\overline{\text{FLOW_CONN}}$ INPUTS
04–26–04 CHANGED LABELS FOR SECONDARY LIMITS – AT STAGE THEY ARE $\overline{\text{FWD_RET_2ND}}$ AND $\overline{\text{FWD_DEP_2ND}}$ AFTER INTERLOCKS THAY ARE $\overline{\text{2RET}}$ AND $\overline{\text{2DPL}}$
05–05–04 CHANGED E–STOP AND EMERGENCY STOP TO HIGH TRUE LOGIC AND RENAMED LOCAL/REMOTE SWITCH
05–27–04 REMOVED EMERGENCY NULL PADDLE INPUTS AT BITS 62 AND 63 AND ADDED EMERGENCY NULL MODE INPUT AT BIT 68
06–15–04 REWORKED FOR MANUAL PADDLE WIRING
10–13–04 ADDED I/O– AND OUT– COMMON PINS. ADDED PINS 1–4
10–25–04 CORRECTED GND CONNECTIONS AT PINS 1 AND 3 AND REMOVED +5V CONNECTION (5v COMES FROM AMP–19520)
02–07–05 CORRECTED SIGNAL CONNECTIONS FROM J405 TO J701 (J701 IS THE CONNECTOR ON THE I/O PANEL AND J405 IS ON THE INTERLOCK PANEL)

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	ADC EXTENDED I/O SIGNALS AND WIRING KECK ADC

DES'N BY: B. Alcott	ORIGIN DATE: 02–11–04	DWG. NO. EL–3608	NUM. 2 OF 3
Last SN	MODIFY DATE: 02–07–05		REV. A
PRINT TIME: 07:34:04	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC\		ADC_in_out.sch	

ADC EXTENDED I/O BITS 17 – 48 HIGH CURRENT DRIVERS

	BIT	PIN	I/O	SIGNAL	FUNCTION	TO
BLOCK 2, BANK 0	PWROUT17	104	O	–	–	–
	PWROUT18	103	O	–	–	–
	PWROUT19	102	O	–	–	–
	PWROUT20	101	O	–	–	–
	PWROUT21	100	O	–	–	–
	PWROUT22	99	O	–	–	–
	PWROUT23	98	O	–	–	–
	PWROUT24	97	O	–	–	–
		96		I/OC17–24	+5V	–
		95		OUTC17–24	–	–
BLOCK 3, BANK 1	PWROUT25	84	O	–	+5V	–
	PWROUT26	83	O	–	–	–
	PWROUT27	82	O	–	–	–
	PWROUT28	81	O	–	–	–
	PWROUT29	80	O	–	–	–
	PWROUT30	79	O	–	–	–
	PWROUT31	78	O	–	–	–
	PWROUT32	77	O	–	–	–
		76		I/OC25–32	–	–
		75		OUTC25–32	–	–

HIGH CURRENT DRIVERS CAN BE USED BY BANKS OF 8
NORMAL I/O AND POWER OUTPUTS ARE MUTUALLY EXCLUSIVE

NOTES: 1) I/O BIT NUMBERS STARTING WITH A 'P' DENOTE POWER DRIVER ABILITY

2) AS PER GALIL APP. NOTE #1438, TO USE BANKS 0 AND 1 FOR INPUTS, THE IOM–1964 CONNECTION LABELED OUTCn MUST BE CONNECTED TO THE ISOLATED POWER SUPPLY GROUND.

B

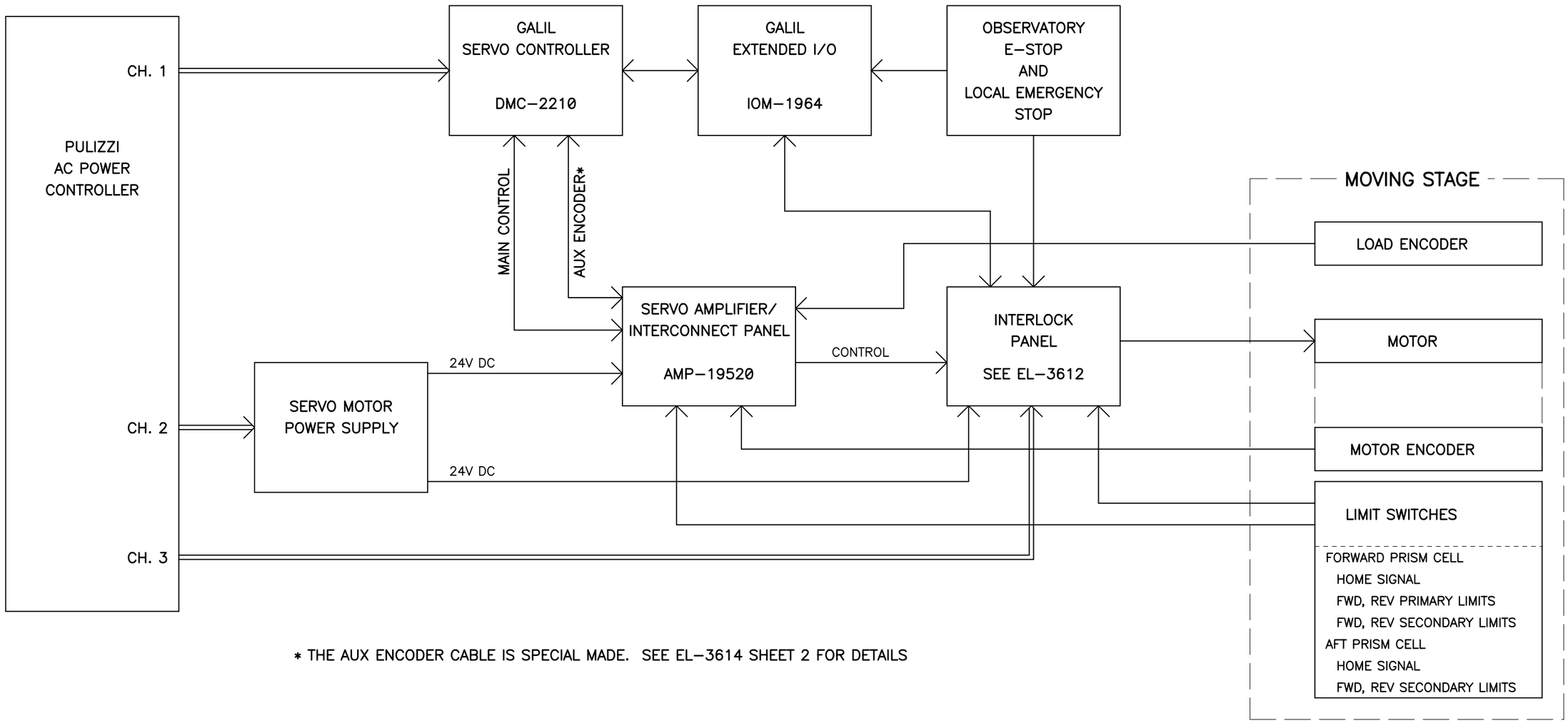
REVISIONS

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

ADC EXTENDED I/O
SIGNALS AND WIRING
KECK ADC

DES'N BY: B. Alcott	ORIGIN DATE: 02–11–04	DWG. NO. EL–3608	NUM. 3 OF 3
Last SN	MODIFY DATE:		REV. A
PRINT TIME: 11:11:11	PRINT DATE: Thu Oct 14, 2004		
PATH: ADC\		ADC_in_out.sch	

NUM. 3 OF 3
ADC EXTENDED I/O SIGNALS AND WIRING BITS 17–48
EL–3608



* THE AUX ENCODER CABLE IS SPECIAL MADE. SEE EL-3614 SHEET 2 FOR DETAILS

B

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_power_sh_1.sch.pdf

02-19-04 ADDED NEW SHEETS 2 AND 3
03-23-04 REARRANGED BLOCKS AND ADDED SHEET 6 FOR EMERGENCY NULL PADDLE WIRING
04-14-04 MOVED LOAD ENCODER CONNECTION FROM INTERLOCK BOX TO SERVO AMPLIFIER AND ADDED AUXILIARY ENCODER CABLE BETWEEN CONTROLLER AND AMPLIFIER
04-20-04 RENUMBERED ALL CONNECTORS
04-20-04 REMOVED J405 AND J406 AND RENUMBERED J407 TO J405 AND J408 TO J406. SHEETS 2 & 3
05-05-04 MADE SIGNAL NAME CHANGES TO SHEETS 2, 3, AND 5
11-24-04 UPDATED SHEET 2 FOR +24V POWER SUPPLY MONITORING

UNIVERSITY OF CALIFORNIA
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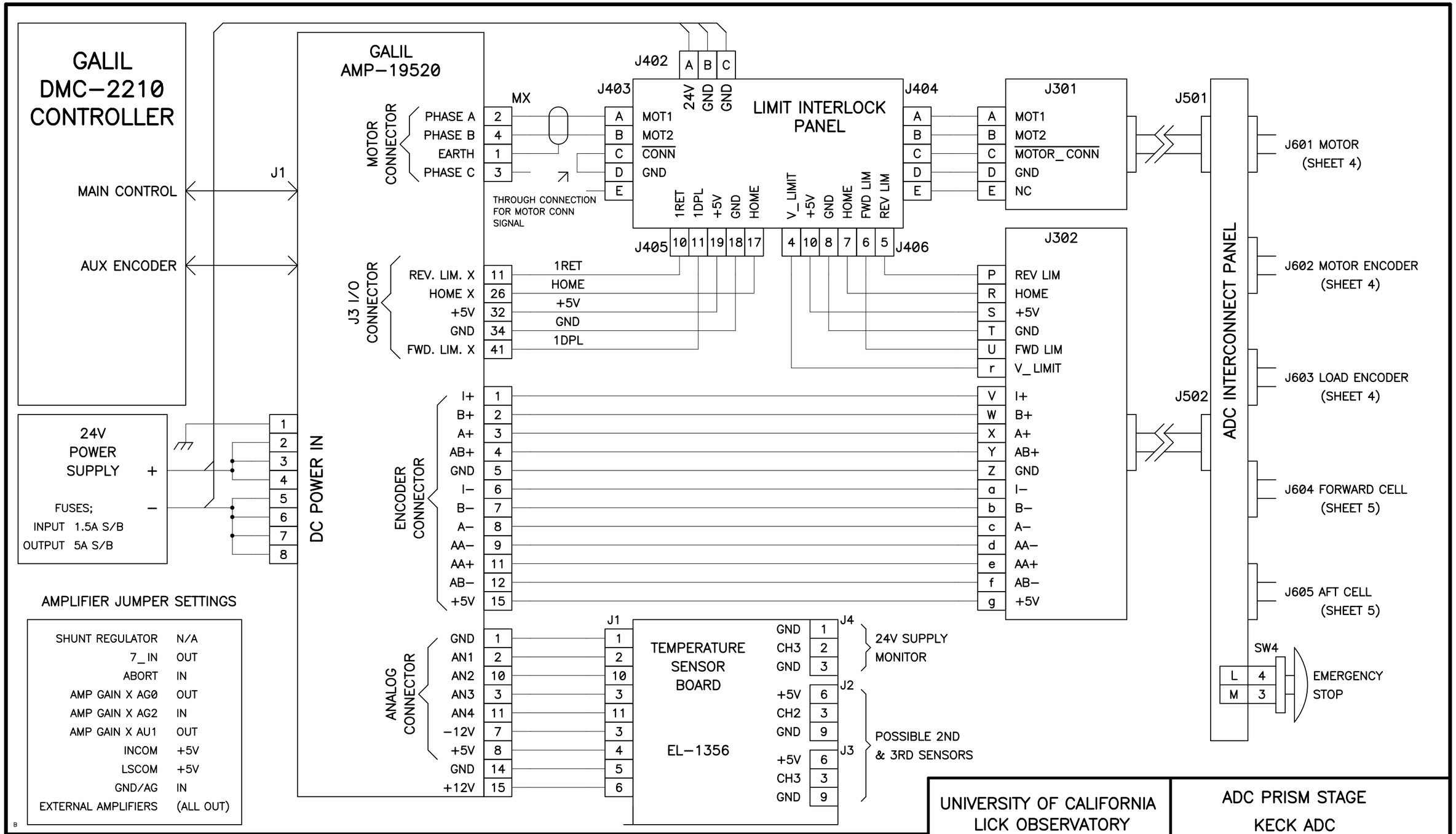
ADC PRISM STAGE
KECK ADC

DES'N BY: B. Alcott	ORIGIN DATE: 09-16-03	DWG. NO. EL-3610	NUM. 1 OF 6
Last SN	MODIFY DATE: 11-24-04		REV. A
PRINT TIME: 11:46:43	PRINT DATE: Wed Feb 09, 2005		
PATH: ADC\		ADC_stage.sch	

NUM. 1 OF 6

ADC STAGE WIRING

EL-3610



AMPLIFIER JUMPER SETTINGS

SHUNT REGULATOR	N/A
7_IN	OUT
ABORT	IN
AMP GAIN X AG0	OUT
AMP GAIN X AG2	IN
AMP GAIN X AU1	OUT
INCOM	+5V
LSCOM	+5V
GND/AG	IN
EXTERNAL AMPLIFIERS	(ALL OUT)

B

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_power_sh_2.sch.pdf

04-16-04 ADDED PIN NUMBERS TO J202
04-20-04 RENUMBERED ALL CONNECTORS
04-23-04 REMOVED CONNECTORS J405 AND J406 AND ADDED J403 CONNECTION FROM PIN C TO PIN D
04-26-04 ADDED NOTE FOR PRIMARY LIMIT +5V
06-14-04 CORRECTED LABELS AT CONNECTOR J301
06-17-04 CORRECTED PIN NUMBERS OF J405 AND J405. ADDED CONNECTOR J402 LABEL TO 24V INPUT
10-14-04 ADDED EMERGENCY STOP SWITCH
11-24-04 ADDED 4TH ANALOG INPUT FROM TEMPERATURE SENSOR BOARD (AN4) FOR UPDATED BOARD WITH +24V POWER SUPPLY MONITORING

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

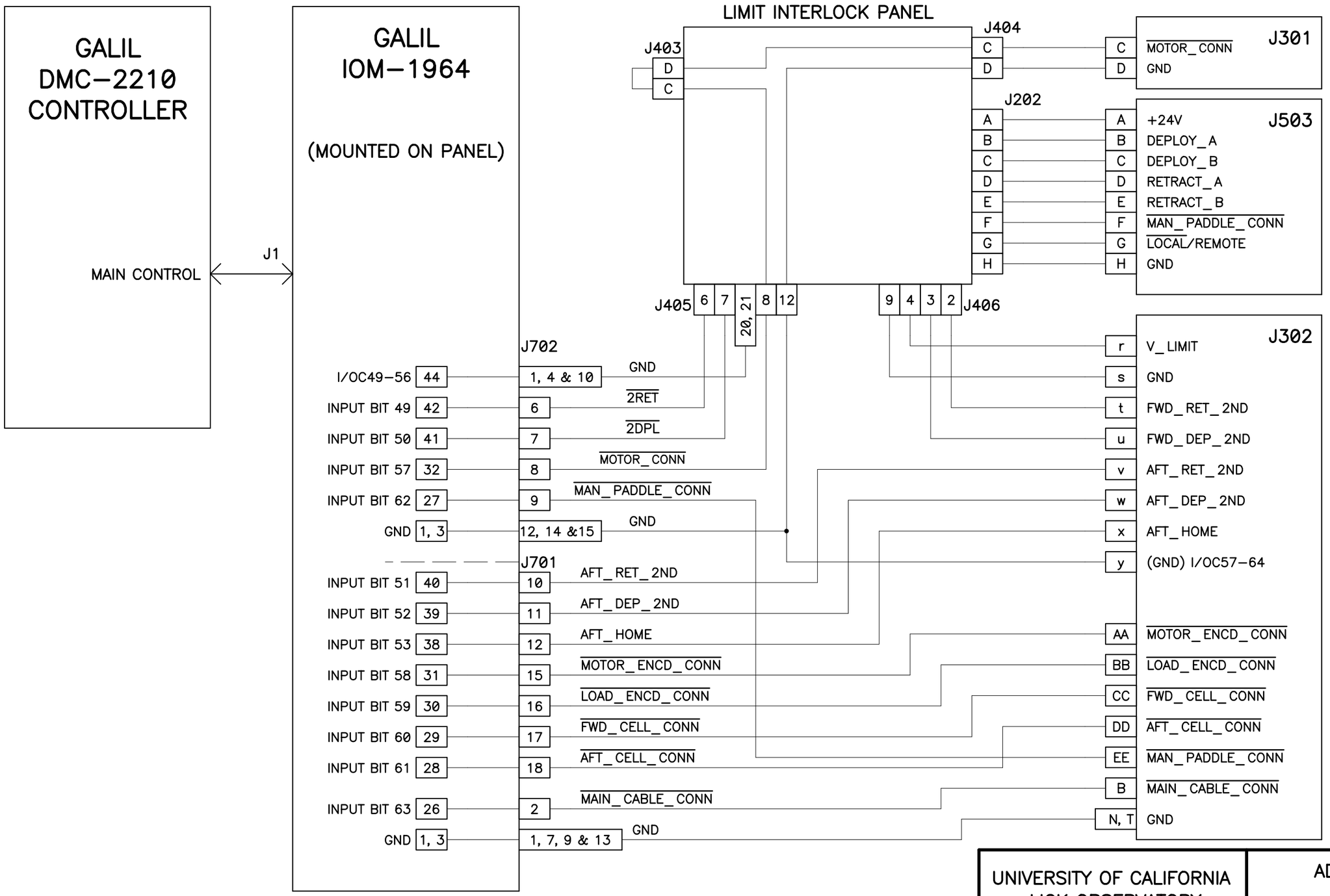
ADC PRISM STAGE
KECK ADC

DES'N BY: B. Alcott	ORIGIN DATE: 09-16-03	DWG. NO. EL-3610	NUM. 2 OF 6
Last SN	MODIFY DATE: 11-24-04		REV. A
PRINT TIME: 13:58:46	PRINT DATE: Fri Feb 11, 2005		
PATH: ADC\		ADC_stage.sch	

NUM. 2 OF 6

ADC STAGE WIRING

EL-3610



B

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_power_sh_3.sch.pdf

04-16-04 ADDED PIN NUMBERS TO J202
04-20-04 RENUMBERED ALL CONNECTORS
04-22-04 REWORKED SECONDARY LIMIT SIGNALS
06-14-04 REARRANGED MOTOR_CONN CONNECTIONS AT J301 AND J404
02-07-05 ADDED CONNECTORS J701 AND J702 THAT LIVE ON I/O MOUNTING PANEL AND CORRECTED VARIOUS PIN NUMBERS

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

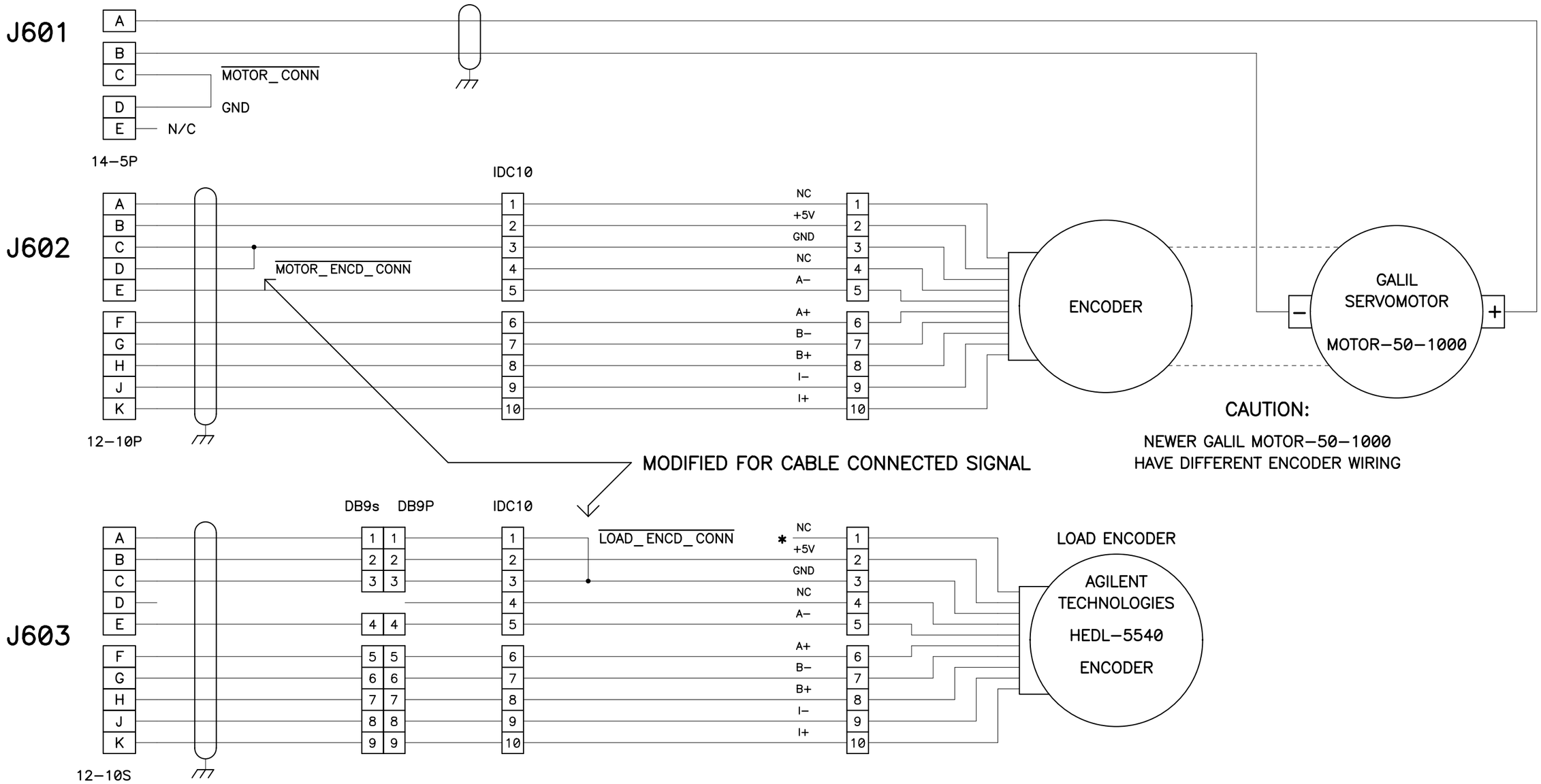
ADC PRISM STAGE
KECK ADC

DES'N BY: B. Alcott	ORIGIN DATE: 09-16-03	DWG. NO. EL-3610	NUM. 3 OF 6
Last SN	MODIFY DATE: 02-07-05		REV. A
PRINT TIME: 07:31:31	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC\		ADC_stage.sch	

NUM. 3 OF 6

ADC STAGE WIRING

EL-3610



*ENCODER MODIFICATIONS:

TO ENSURE THAT THE ENCODER CONNECTED SIGNALS REMAIN UNIQUE, THE MOTOR AND LOAD ENCODER WIRING HASE BEEN MODIFIED. IN EACH CASE, THE GND SIGNAL COMING INTO THE ENCODER HAS BEEN WIRED BACK TO ONE OF TWO UNUSED PINS. THESE PINS ARE THEN WIRED BACK TO TWO OF THE CONTROLLER'S EXTENDED I/O INPUTS. THIS ALLOWS THE CONTROLLER TO DETERMINE IF EITHER ENCODER IS DISCONNECTED.

B

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_power_sh_4.sch.pdf

04–20–04 RENUMBERED ALL CONNECTORS
02–15–05 ADDED DB9 CONNECTOR FOR LOAD ENCODER
03–22–05 CORRECTED MOTOR LEAD WIRING (SWAPPED + AND –) AND REMOVED DB–9 CONNECT FROM MOTOR ENCODER WIRING

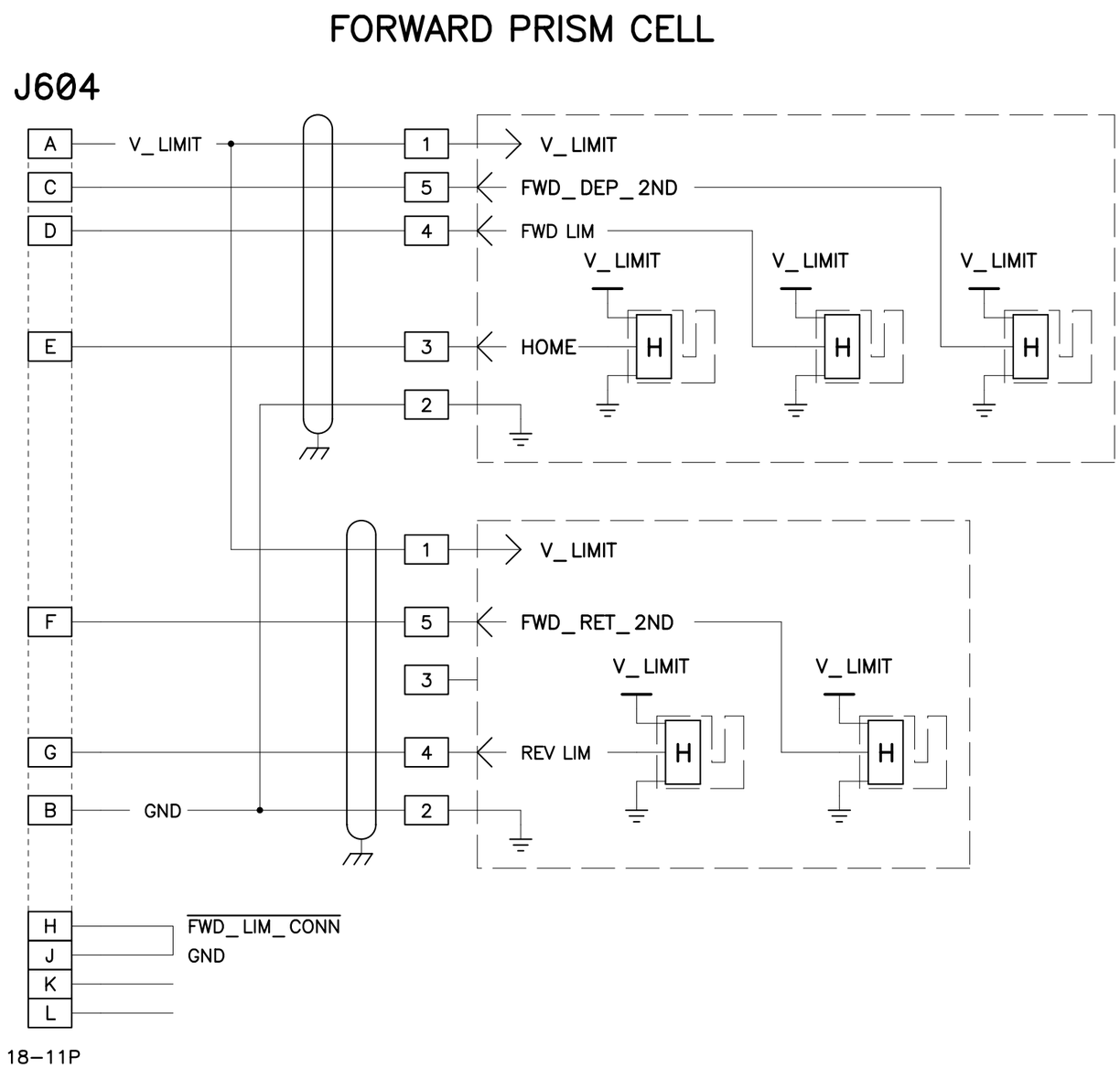
UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	ADC PRISM STAGE KECK ADC

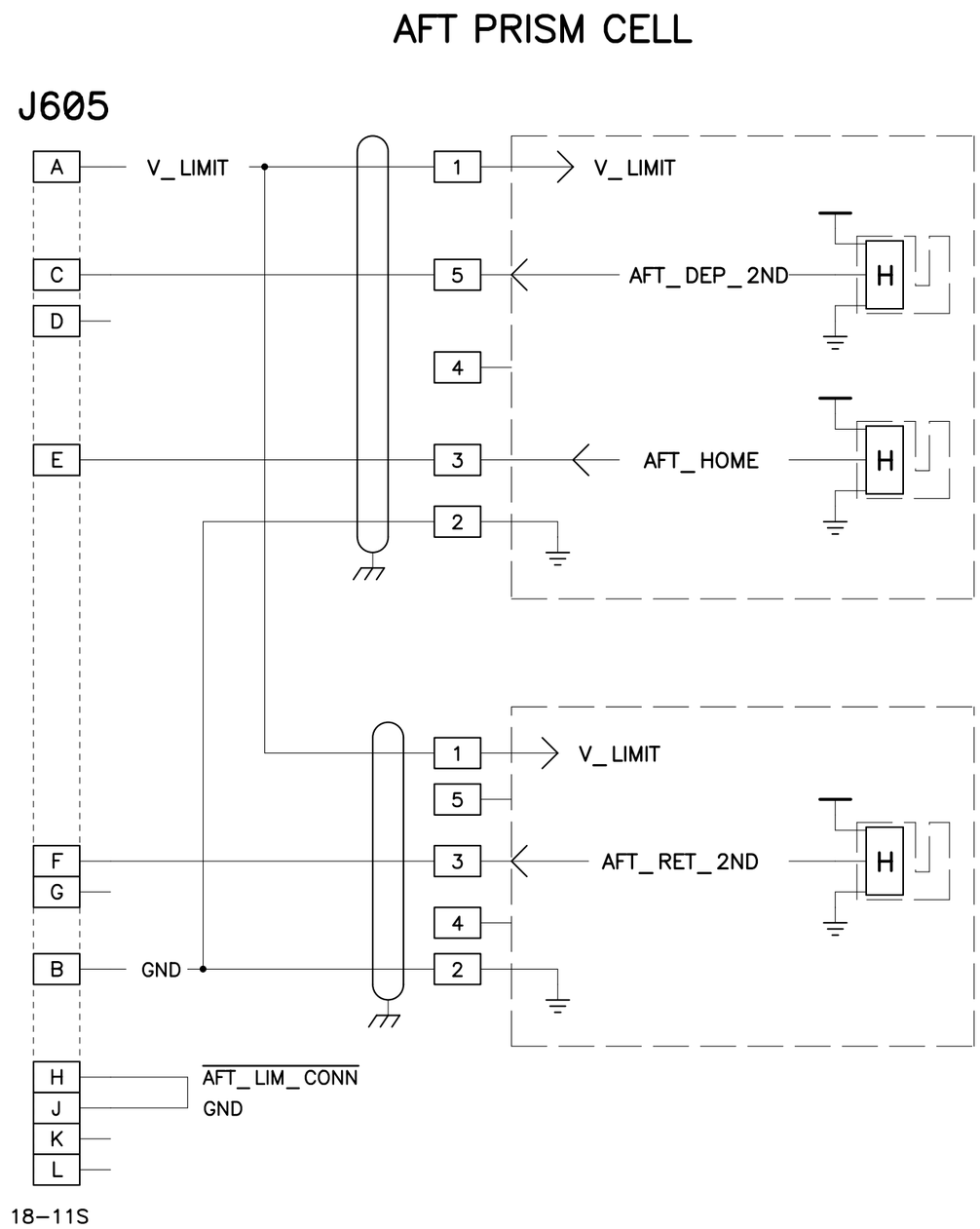
DES'N BY: B. Alcott	ORIGIN DATE: 09–16–03	DWG. NO. EL–3610	NUM. 4 OF 6
Last SN	MODIFY DATE: 03–22–05		REV. A
PRINT TIME: 07:31:43	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC\		ADC_stage.sch	

NUM. 4 OF 6

ADC STAGE WIRING

EL–3610





ALL SENSORS:
CHERRY VN101501
OR VN101503

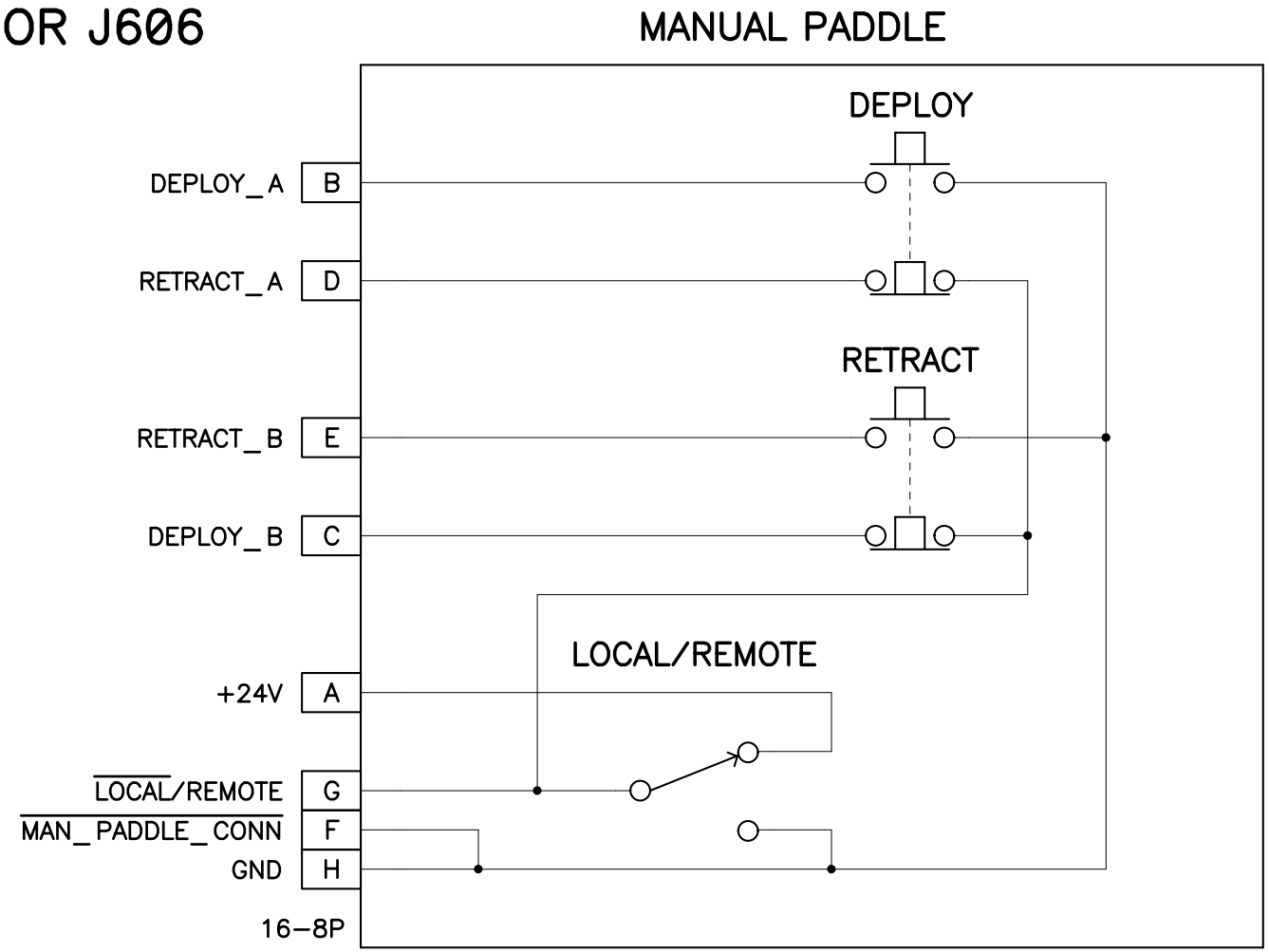
B

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_power_sh_5.sch.pdf

04-20-04 RENUMBERED ALL CONNECTORS
04-26-04 CHANGE J604-A FROM +5V TO FWD_2ND_PWR. THIS POWER IS SWITCHED FROM GALIL +5V TO INTERLOCK +15V WHEN SYSTEM IS IN BYPASS MODE.
05-05-04 REMOVED BAR (LOW TRUE) FROM HALL-EFFECT SIGNAL NAMES
06-21-04 CHANGED LABEL FOR FWD CELL POWER FROM FWD_2ND_PWR/Vcc TO V_LIMIT
10-25-04 CORRECTED J604 AND J605 LAST PIN LABEL FROM J TO L
02-24-05 REARRANGED PAGE, BROKE SENSOR UP BY BOARDS
03-22-05 SWAPPED GENDERS ON CONNECTORS J604 AND J605 TO REFLECT AS WIRED

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		ADC PRISM STAGE KECK ADC	
DES'N BY: B. Alcott	ORIGIN DATE: 09-16-03	DWG. NO. EL-3610	NUM. 5 OF 6
Last SN	MODIFY DATE: 03-22-05		REV. A
PRINT TIME: 07:31:53	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC\		ADC_stage.sch	



http://loel.ucolick.org/manual/ADC/schematics/ADC_power_sh_6.sch.pdf

REVISION
03-23-04 ADDED THIS SHEET
04-20-04 RENUMBERED ALL CONNECTORS
06-09-04 REDREW AS MANUAL CONTROL PADDLE
10-25-04 ADDED SWITCH LABELS
02-09-05 UPDATED PADDLE WIRING

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		ADC PRISM STAGE KECK ADC	
DES'N BY: B. Alcott	ORIGIN DATE: 09-16-03	DWG. NO.	NUM. 6 OF 6
Last SN	MODIFY DATE: 02-09-05	EL-3610	REV. A
PRINT TIME: 07:30:48	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC\		ADC_stage.sch	

MAIN SIGNAL CABLE (J302 AND J502)

BOX MOUNT: MS3122E22–55S
STRAIGHT PLUG: MS3126F22–55P

PIN	TO: J302	TO: J502	SIGNAL	FUNCTION
A	IOM PIN–34	–	I/OC57–64	GND
B	IOM PIN–26	–	MAIN_CABLE_CONN	I/O BIT 63
C	–	–	–	–
D	–	–	–	–
E	–	–	–	–
F	–	–	–	–
G	–	J604–K	–	(UNASSIGNED SPARES)
H	–	J604–L	–	(UNASSIGNED SPARES)
J	–	J605–K	–	(UNASSIGNED SPARES)
K	–	J605–L	–	(UNASSIGNED SPARES)
L	J406–8	SW4–4	EMERGENCY_STOP	STOP BUTTON PUSHED
M	J406–10	SW4–3	GND	EMERGENCY STOP SWITCH
N	IOM PIN–24	–	GND	IO COMMON 65–72
P	J406–5	J604–G	REV_LIM	ADC STAGE REVERSE LIMIT
R	J406–7	J604–E	HOME	ADC STAGE HOME POSITION
S	IOM–2	J605–A	+5V	+5V
T	IOM–1	J605–B,J J604–B,J	GND	GND (ENCODERS)
U	J406–6	J604–D	FWD_LIM	ADC STAGE FORWARD LIMIT
V	AMP DB15 X–1	J602–K	I+	MAIN ENCODER I+
W	AMP DB15 X–2	J602–H	B+	MAIN ENCODER B+
X	AMP DB15 X–3	J602–F	A+	MAIN ENCODER A+
Y	AMP DB15 X–4	J603–H	AB+	AUXILIARY ENCODER B+
Z	AMP DB15 X–5	J602–C, J603–C	GND	GND
a	AMP DB15 X–6	J602–J	I–	MAIN ENCODER I–
b	AMP DB15 X–7	J602–G	B–	MAIN ENCODER B–
c	AMP DB15 X–8	J602–E	A–	MAIN ENCODER A–
d	AMP DB15 X–9	J603–E	AA–	AUXILIARY ENCODER A–
e	AMP DB15 X–11	J603–F	AA+	AUXILIARY ENCODER A+
f	AMP DB15 X–12	J603–G	AB–	AUXILIARY ENCODER B–
g	AMP DB15 X–15	J602–B, J603–B	+5V	+5V

PIN	TO: J302	TO: J502	SIGNAL	FUNCTION
h	–	–	–	–
i	INTERLOCKS	–	24V RTN	24V GND
j	–	–	–	–
k	–	–	–	–
m	–	–	–	–
n	–	–	–	–
p	J406–1	–	GND	GND
q	–	–	–	–
r	J406–4	J604–A	V_LIMIT	POWER FOR LIMITS
s	J406–9	J604–B	GND	GND
t	J406–2	J604–F	FWD_RET_2ND	SECONDARY LIMIT
u	J406–3	J604–C	FWD_DEP_2ND	SECONDARY LIMIT
v	IOM PIN–40	J605–F	AFT_RET_2ND	I/O BIT 51
w	IOM PIN–39	J605–C	AFT_DEP_2ND	I/O BIT 52
x	IOM PIN–38	J605–E	AFT_HOME	I/O BIT 53
y	IOM PIN–34	–	COM 57–64	COMMON FOR I/O BITS 57–64
z	–	–	–	–
AA	IOM PIN–31	J602–D	MOTOR_ENCD_CONN	I/O BIT 58
BB	IOM PIN–30	J603–A	LOAD_ENCD_CONN	I/O BIT 59
CC	IOM PIN–29	J604–H	FWD_CELL_CONN	I/O BIT 60
DD	IOM PIN–28	J605–H	AFT_CELL_CONN	I/O BIT 61
EE	–	–	–	–
FF	–	–	–	–
GG	–	–	–	–
HH	–	–	–	–

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_stage_cables_SH1.sch.pdf

04–21–04 ADDED SECOND SHEET
04–26–04 REMOVED DUPLICATE SIGNAL REMOTE_STOP_CONN FROM PIN GG
04–28–04 ADDED CONNECTOR PART NUMBERS
05–05–04 CHANGED SIGNAL SENSE OF THE HALL–EFFECT OUTPUTS – OUTPUT HIGH WHEN SWITCH IS BLOCKED – ALL SHEETS
06–09–04 REMOVED NULL PADDLE SIGNALS THAT NO LONGER EXIST
10–14–04 ADDED GROUNDS AT PINS M, GG, AND HH. CORRECTED EMERGENCY_STOP SIGNAL DESTIONATION (J406–8)

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KECK ADC
STAGE CABLES

DES'N BY: B. Alcott	ORIGIN DATE: 04–14–04	DWG. NO. EL–3611	NUM. 1 OF 3
Last SN	MODIFY DATE: 10–14–04		REV. A
PRINT TIME: 11:24:31	PRINT DATE: Thu Oct 14, 2004		
PATH: ADC\		ADC_stage_cables.sch	

NUM. 1 OF 3

KECK ADC STAGE CABLES

EL–3611

MAIN MOTOR CABLE (J404, J301, J501,J601)

BOX MOUNT: MS3122E14–5S
STRAIGHT PLUG: MS3126F14–5P

PIN	TO	SIGNAL	FUNCTION
A	J601–A	MOT1	MOTOR POWER
B	J601–B	MOT2	MOTOR POWER
C	J601–C	$\overline{\text{MOTOR_CONN}}$	MOTOR CABLE CONNECTED SIGNAL
D	J601–D	GND	GND
E	J601–E	–	–

MOTOR ENCODER CABLE (J602)

BOX MOUNT: MS3122E12–10S
STRAIGHT PLUG: MS3126F12–10P

PIN	TO	SIGNAL	FUNCTION
A	–	–	NC
B	J502–g	+5V	+5V
C	J502–Z	GND	GND
D	J502–AA	$\overline{\text{MOTOR_ENCD_CONN}}$	MOTOR ENCODER CABLE CONNECTED
E	J502–c	A–	MAIN ENCODER A–
F	J502–X	A+	MAIN ENCODER A+
G	J502–b	B–	MAIN ENCODER B–
H	J502–W	B+	MAIN ENCODER B+
J	J502–a	I–	MAIN ENCODER INDEX–
K	J502–V	I+	MAIN ENCODER INDEX+

LOAD ENCODER CABLE (J603)

BOX MOUNT: MS3122E12–10P
STRAIGHT PLUG: MS3126F12–10S

PIN	TO	SIGNAL	FUNCTION
A	J502–BB	$\overline{\text{LOAD_ENCD_CONN}}$	LOAD ENCODER CABLE CONNECTED
B	J502–g	+5V	+5V
C	J502–Z	GND	GND
D	–	–	NC
E	J502–d	AA–	AUXILIARY ENCODER A–
F	J502–e	AA+	AUXILIARY ENCODER A+
G	J502–f	AB–	AUXILIARY ENCODER B–
H	J502–Y	AB+	AUXILIARY ENCODER B+
J	NC	NC	AUXILIARY ENCODER INDEX–
K	NC	NC	AUXILIARY ENCODER INDEX+

FORWARD PRISM CELL LIMITS (J604)

BOX MOUNT: MS3122E18–11S
STRAIGHT PLUG: MS3126F18–11P

PIN	TO	SIGNAL	FUNCTION
A	J502–S	V_LIMIT	V_LIMIT
B	J502–s	GND	GND
C	J502–u	FWD_DEP_2ND	FORWARD CELL DEPLOY SECONDARY
D	J502–U	FWD_LIM	FORWARD LIMIT (DEPLOYED)
E	J502–R	HOME	FORWARD CELL HOME SIGNAL
F	J502–t	FWD_RET_2ND	FORWARD CELL RETRACT SECONDARY
G	J502–P	REV_LIM	REVERSE LIMIT (RETRACT)
H	J502–CC	FWD_CELL_CONN	FORWARD CELL CABLE CONNECTED
J	J502–T	GND	GND
K	J502–G	–	–
L	J502–H	–	–

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_stage_cables_SH2.sch.pdf

05–05–04 CHANGED SIGNAL SENSE OF THE HALL–EFFECT OUTPUTS – OUTPUT HIGH WHEN SWITCH IS BLOCKED – ALL SHEETS
06–14–04 CORRECTED MAIN MOTOR CABLE WIRING PINOUT

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LICK OBSERVATORY

KECK ADC
STAGE CABLES

DES'N BY: B. Alcott	ORIGIN DATE: 04–14–04	DWG. NO. EL–3611	NUM. 2 OF 3
Last SN	MODIFY DATE: 06–14–04		REV. A
PRINT TIME: 11:18:25	PRINT DATE: Thu Oct 14, 2004		
PATH: ADC\		ADC_stage_cables.sch	

KECK ADC STAGE CABLES

EL–3611

AFT PRISM CELL LIMITS (J605)

BOX MOUNT: MS3122E18–11P
STRAIGHT PLUG: MS3126F18–11S

PIN	TO	SIGNAL	FUNCTION
A	J502–S	+5V	+5V
B	J502–T	GND	GND
C	J502–w	AFT_DEP_2ND	AFT CELL DEPLOY SECONDARY
D	–	–	–
E	J502–x	AFT_HOME	AFT CELL HOME SIGNAL
F	J502–v	AFT_RET_2ND	AFT CELL RETRACT SECONDARY
G	–	–	–
H	J502–DD	$\overline{\text{AFT_CELL_CONN}}$	AFT CELL CABLE CONNECTED
J	J502–T	GND	GND
K	J502–J	–	–
L	J502–K	–	–

MANUAL PADDLE CABLE (J202, J303, J503, J606)

BOX MOUNT: MS3122E16–8P
STRAIGHT PLUG: MS3126F16–8S

PIN	TO	SIGNAL	FUNCTION
A	–	+24V	+24V
B	–	DEPLOY_A	DEPLOY SIGNAL
C	–	DEPLOY_B	DEPLOY SIGNAL
D	–	RETRACT_A	RETRACT SIGNAL
E	–	RETRACT_B	RETRACT SIGNAL
F	–	$\overline{\text{MAN_PADDLE_CONN}}$	MANUAL PADDLE CONNECTED SIGNAL
G	–	$\overline{\text{LOCAL}}$/REMOTE	LOCAL CONTROL SIGNAL
H	–	GND	GND

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_stage_cables_SH2.sch.pdf

05–05–04 CHANGED SIGNAL SENSE OF THE HALL–EFFECT OUTPUTS – OUTPUT HIGH WHEN SWITCH IS BLOCKED – ALL SHEETS
06–09–04 CHANGED EMERGENCY NULL PADDLE TO MANUAL CONTROL PADDLE

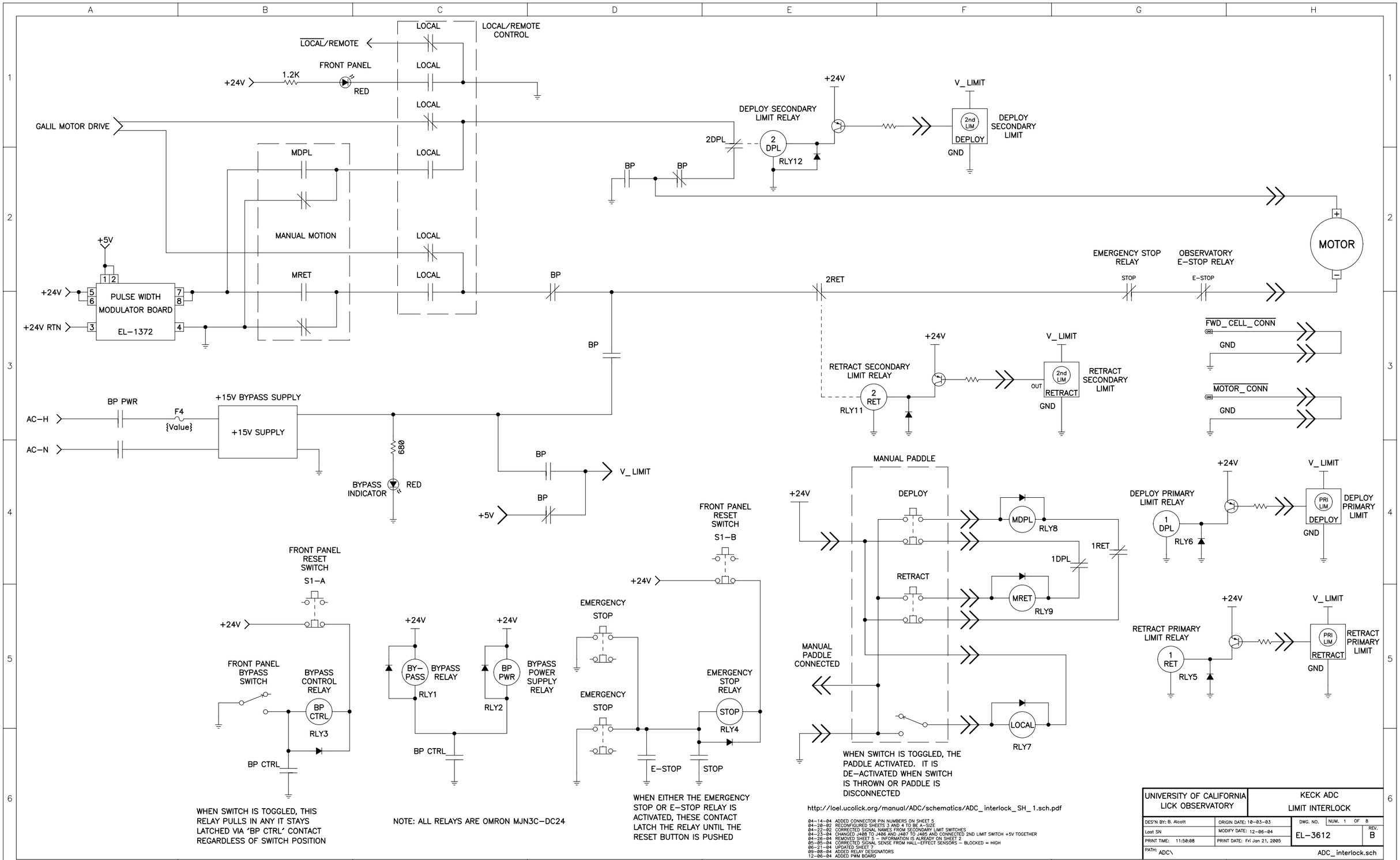
UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

KECK ADC
STAGE CABLES

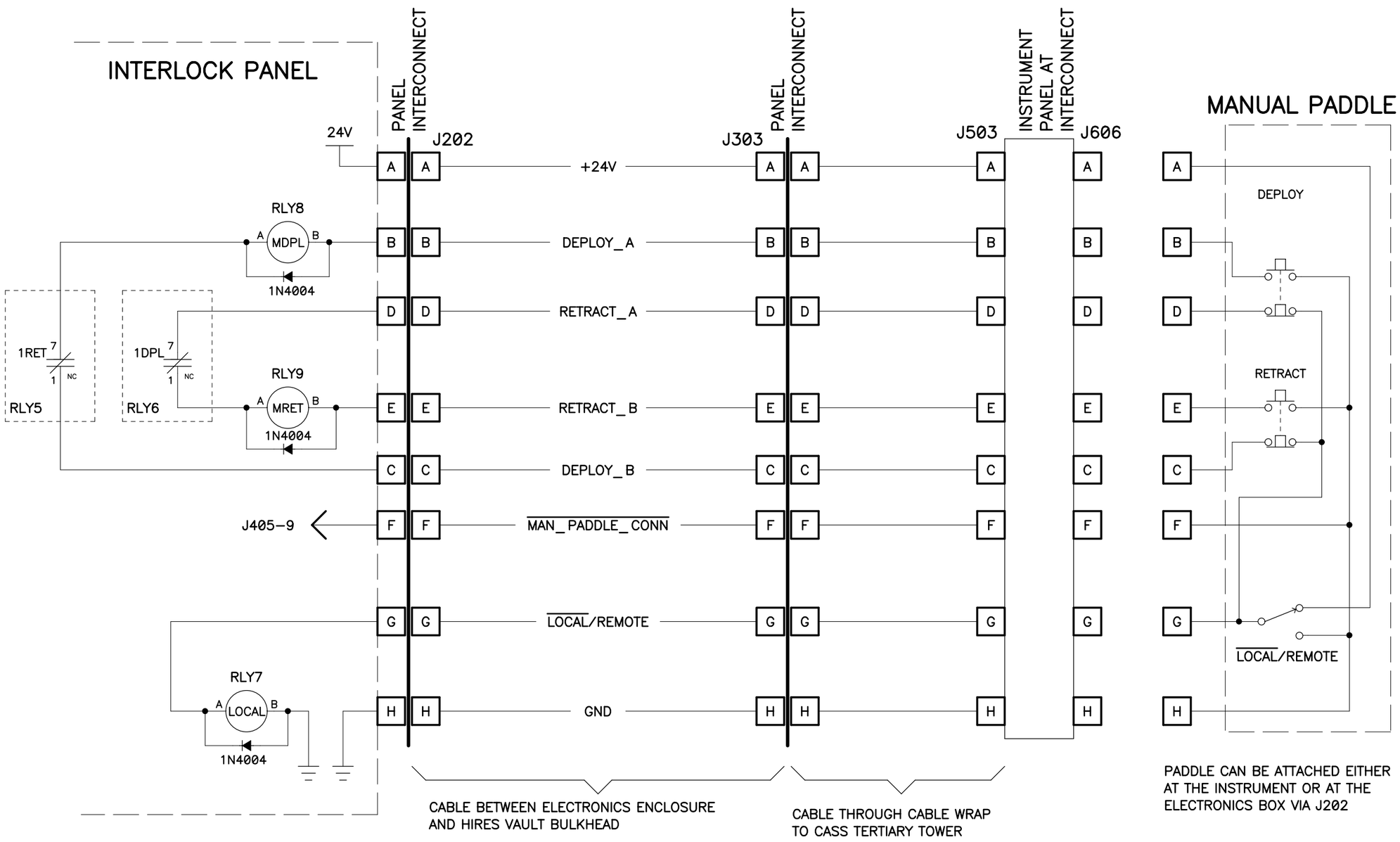
DES'N BY: B. Alcott	ORIGIN DATE: 04–14–04	DWG. NO. EL–3611	NUM. 3 OF 3 REV. A
Last SN	MODIFY DATE: 06–09–04		
PRINT TIME: 11:18:31	PRINT DATE: Thu Oct 14, 2004		
PATH: ADC\		ADC_stage_cables.sch	

KECK ADC STAGE CABLES

EL–3611


LOCAL/REMOTE
LOCAL/REMOTE CONTROL
LOCAL
FRONT PANEL
+24V
1.2K
RED
GALIL MOTOR DRIVE
MDPL
MANUAL MOTION
MRET
+5V
PULSE WIDTH MODULATOR BOARD
EL-1372
+24V RTN
BP
2DPL
DEPLOY SECONDARY LIMIT RELAY
2 DPL
RLY12
V_LIMIT
2nd LIM
DEPLOY
DEPLOY SECONDARY LIMIT
GND
MOTOR
2RET
EMERGENCY STOP RELAY
STOP
OBSERVATORY E-STOP RELAY
E-STOP
FWD_CELL_CONN
MOTOR_CONN
RETRACT SECONDARY LIMIT RELAY
2 RET
RLY11
OUT
RETRACT
RETRACT SECONDARY LIMIT
BP PWR
F4
{Value}
AC-H
AC-N
+15V BYPASS SUPPLY
+15V SUPPLY
680
BYPASS INDICATOR
RED
MANUAL PADDLE
DEPLOY
RETRACT
MANUAL PADDLE CONNECTED
MDPL
RLY8
1RET
1DPL
MRET
RLY9
LOCAL
RLY7
DEPLOY PRIMARY LIMIT RELAY
1 DPL
RLY6
PRI LIM
DEPLOY PRIMARY LIMIT
RETRACT PRIMARY LIMIT RELAY
1 RET
RLY5
RETRACT PRIMARY LIMIT
FRONT PANEL RESET SWITCH S1-A
FRONT PANEL BYPASS SWITCH
BYPASS CONTROL RELAY
BP CTRL
RLY3
BY-PASS
BYPASS RELAY
RLY1
BP PWR
BYPASS POWER SUPPLY RELAY
RLY2
FRONT PANEL RESET SWITCH S1-B
EMERGENCY STOP
EMERGENCY STOP RELAY
RLY4
E-STOP
WHEN SWITCH IS TOGGLED, THE PADDLE ACTIVATED. IT IS DE-ACTIVATED WHEN SWITCH IS THROWN OR PADDLE IS DISCONNECTED
WHEN SWITCH IS TOGGLED, THIS RELAY PULLS IN ANY IT STAYS LATCHED VIA 'BP CTRL' CONTACT REGARDLESS OF SWITCH POSITION
NOTE: ALL RELAYS ARE OMRON MJN3C-DC24
WHEN EITHER THE EMERGENCY STOP OR E-STOP RELAY IS ACTIVATED, THESE CONTACT LATCH THE RELAY UNTIL THE RESET BUTTON IS PUSHED
http://loel.ucolick.org/manual/ADC/schematics/ADC_interlock_SH_1.sch.pdf
04-14-04 ADDED CONNECTOR PIN NUMBERS ON SHEET 5
04-20-02 RECONFIGURED SHEETS 3 AND 4 TO BE A-SIZE
04-22-02 CORRECTED SIGNAL NAMES FROM SECONDARY LIMIT SWITCHES
04-23-04 CHANGED J488 TO J486 AND J487 TO J485 AND CONNECTED 2ND LIMIT SWITCH +5V TOGETHER
04-26-04 REMOVED SHEET 5 - INFORMATION IS ALREADY ON SHEET 2
05-05-04 CORRECTED SIGNAL SENSE FROM HALL-EFFECT SENSORS - BLOCKED = HIGH
06-21-04 UPDATED SHEET 7
09-08-04 ADDED RELAY DESIGNATORS
12-06-04 ADDED PWM BOARD
UNIVERSITY OF CALIFORNIA LICK OBSERVATORY
KECK ADC LIMIT INTERLOCK
DES'N BY: B. Alcott
ORIGIN DATE: 10-03-03
Last SN
MODIFY DATE: 12-06-04
PRINT TIME: 11:50:08
PRINT DATE: Fri Jan 21, 2005
DWG. NO. EL-3612
NUM. 1 OF 8
REV. B
PATH: ADC\
ADC_interlock.sch
KECK ADC LIMIT INTERLOCK
EL-3612

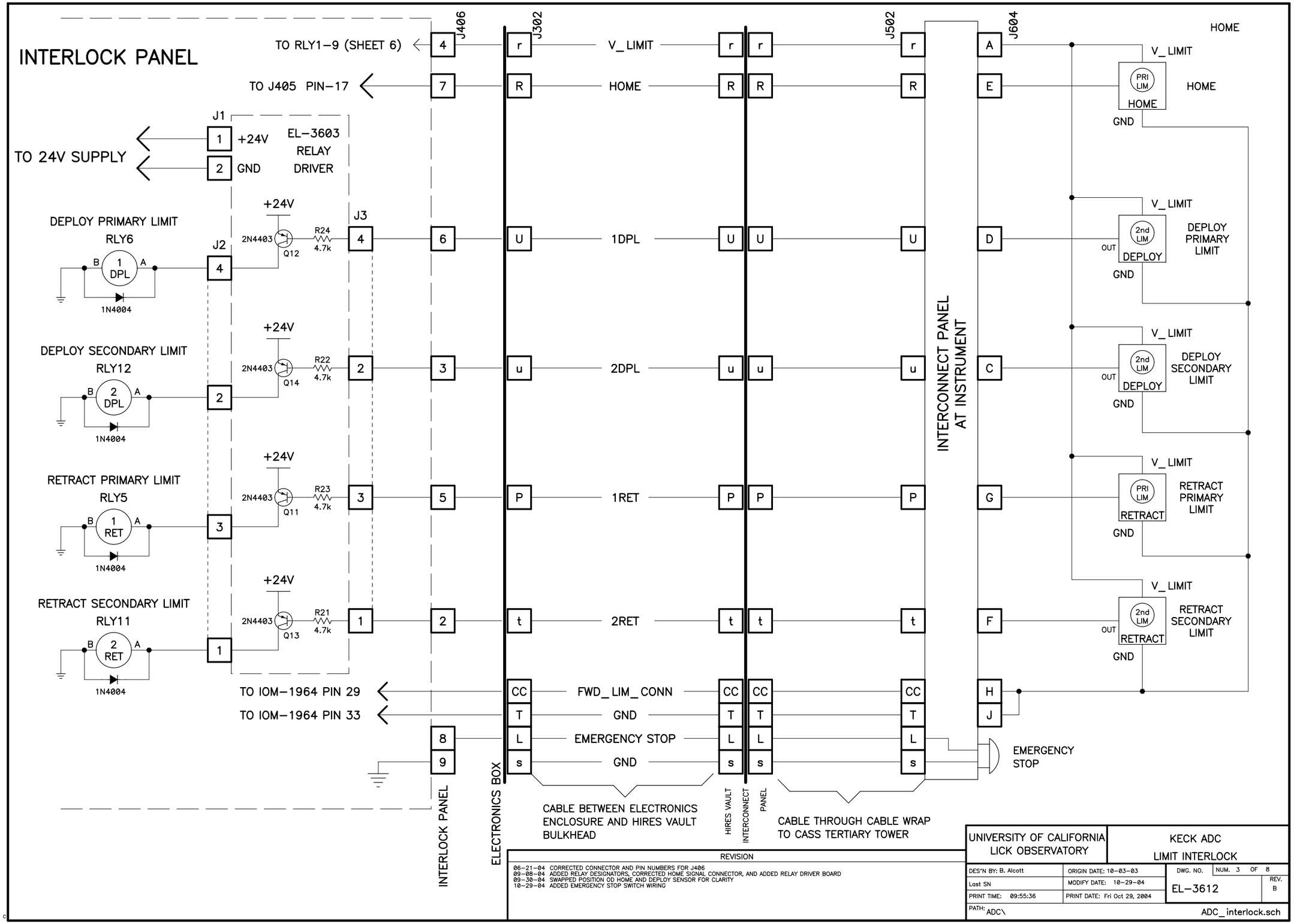
MANUAL PADDLE WIRING DETAILS



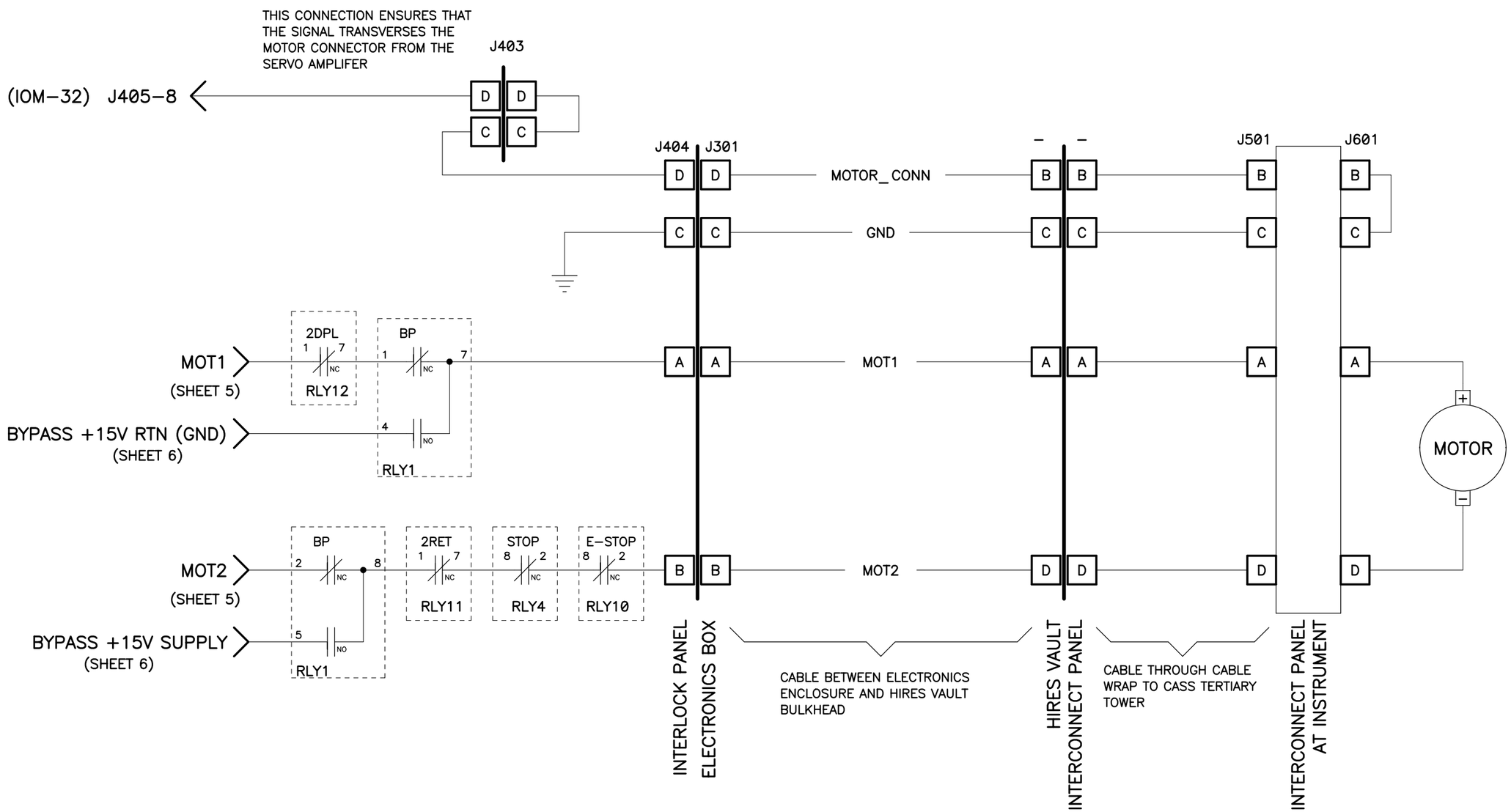
REVISION

09-29-04 ADDED RELAY CONTACT DESIGNATORS
10-12-04 ADDED NO & NC LABELS TO RELAY CONTACTS
10-29-04 CORRECTED MAN_PADDLE_CONN CONNECTION TO J405. CHANGED FROM PIN 7 TO PIN 9
12-21-04 ADDED WIRE FROM LOCAL/REMOTE SWITCH TO +24V
01-05-05 REWIRED +24V LINE INSIDE MANUAL PADDLE

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		KECK ADC LIMIT INTERLOCK	
DES'N BY: B. Alcott	ORIGIN DATE: 10-03-03	DWG. NO. EL-3612	NUM. 2 OF 8
Last SN	MODIFY DATE: 01-05-05		REV. B
PRINT TIME: 11:52:16	PRINT DATE: Fri Jan 21, 2005		
PATH: ADC\		ADC_interlock.sch	


INTERLOCK PANEL
TO RLY1–9 (SHEET 6)
TO J405 PIN–17
TO 24V SUPPLY
J1
1 +24V
2 GND
EL–3603 RELAY DRIVER
DEPLOY PRIMARY LIMIT
RLY6
1 DPL
1N4004
2N4403
Q12
R24 4.7k
DEPLOY SECONDARY LIMIT
RLY12
2 DPL
Q14
R22 4.7k
RETRACT PRIMARY LIMIT
RLY5
1 RET
Q11
R23 4.7k
RETRACT SECONDARY LIMIT
RLY11
2 RET
Q13
R21 4.7k
+24V
J2
J3
TO IOM–1964 PIN 29
TO IOM–1964 PIN 33
INTERLOCK PANEL
ELECTRONICS BOX
J406
J302
J502
J604
V_LIMIT
HOME
1DPL
2DPL
1RET
2RET
FWD_LIM_CONN
GND
EMERGENCY STOP
INTERCONNECT PANEL AT INSTRUMENT
PRI LIM
2nd LIM
DEPLOY
RETRACT
OUT
DEPLOY PRIMARY LIMIT
DEPLOY SECONDARY LIMIT
RETRACT PRIMARY LIMIT
RETRACT SECONDARY LIMIT
EMERGENCY STOP
CABLE BETWEEN ELECTRONICS ENCLOSURE AND HIRES VAULT BULKHEAD
HIRES VAULT INTERCONNECT PANEL
CABLE THROUGH CABLE WRAP TO CASS TERTIARY TOWER
REVISION
06–21–04 CORRECTED CONNECTOR AND PIN NUMBERS FOR J406
09–08–04 ADDED RELAY DESIGNATORS, CORRECTED HOME SIGNAL CONNECTOR, AND ADDED RELAY DRIVER BOARD
09–30–04 SWAPPED POSITION OD HOME AND DEPLOY SENSOR FOR CLARITY
10–29–04 ADDED EMERGENCY STOP SWITCH WIRING
UNIVERSITY OF CALIFORNIA LICK OBSERVATORY
KECK ADC LIMIT INTERLOCK
DES'N BY: B. Alcott
ORIGIN DATE: 10–03–03
Last SN
MODIFY DATE: 10–29–04
PRINT TIME: 09:55:36
PRINT DATE: Fri Oct 29, 2004
DWG. NO. EL–3612
NUM. 3 OF 8
REV. B
PATH: ADC\
ADC_interlock.sch

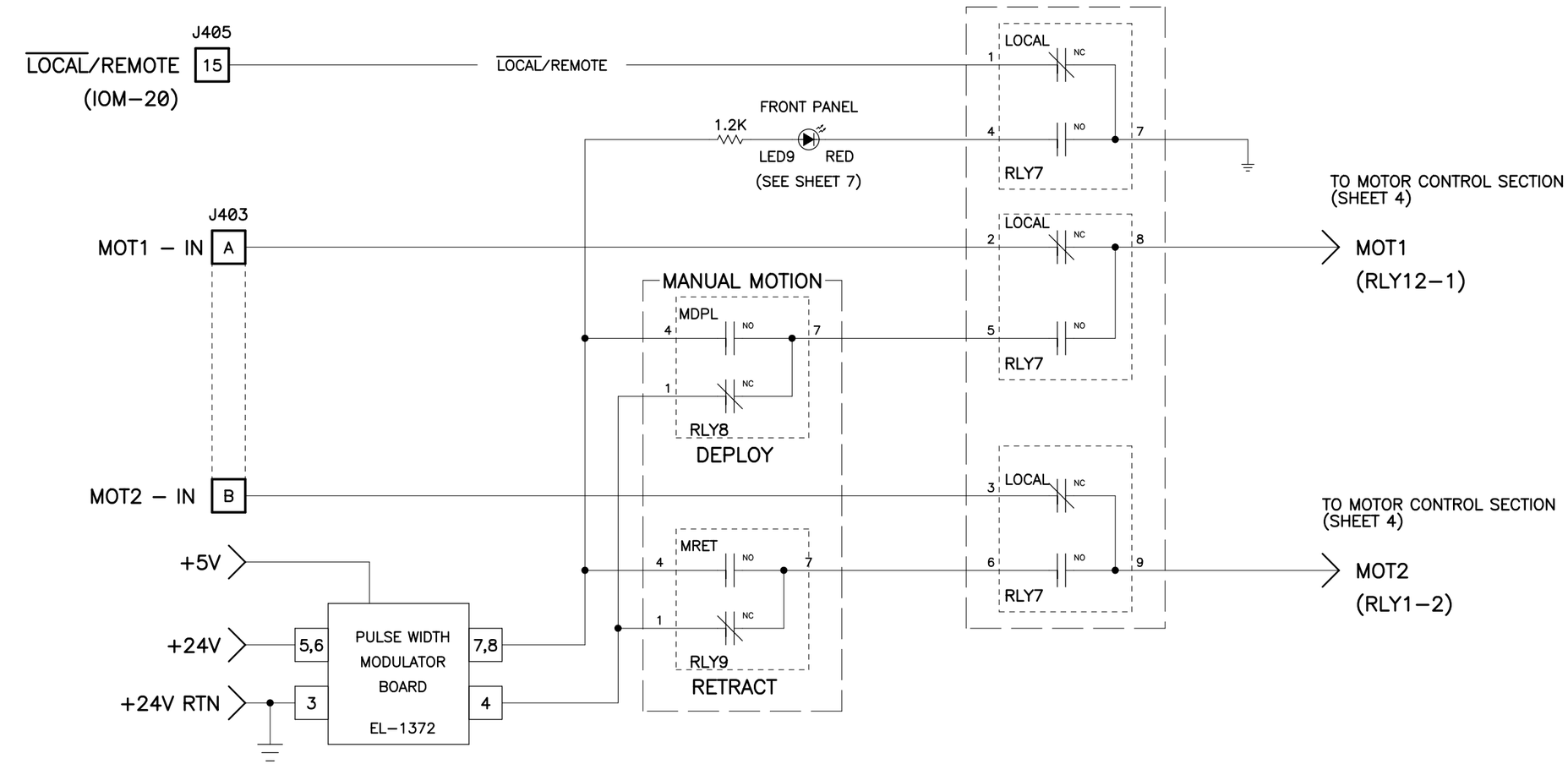
MOTOR WIRING DETAILS



REVISION
09-08-04 ADDED RELAY DESIGNATORS AND CORRECTED MOTOR_ CONN CONNECTOR PIN CALL OUTS
09-29-04 ADDED RELAY CONTACT PIN DESIGNATORS
10-12-04 ADDED NO & NC LABELS TO RELAY CONTACTS

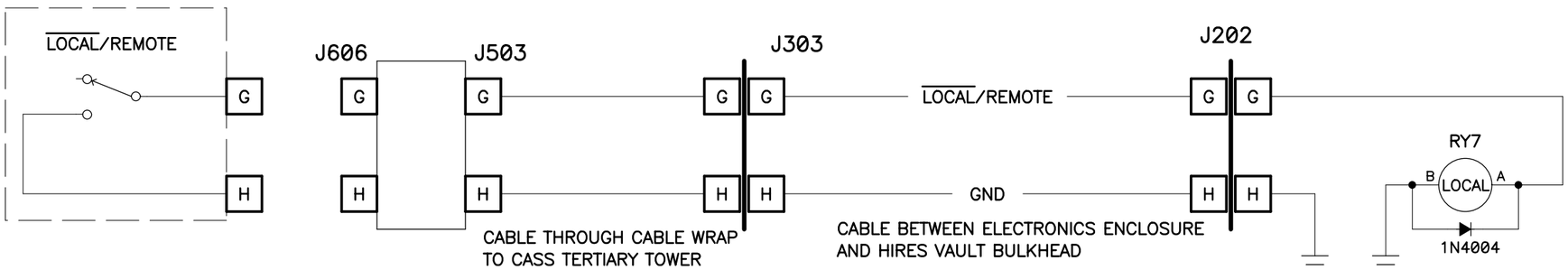
UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		KECK ADC LIMIT INTERLOCK	
DES'N BY: B. Alcott	ORIGIN DATE: 10-03-03	DWG. NO.	NUM. 4 OF 8
Last SN	MODIFY DATE: 09-29-04	EL-3612	REV. B
PRINT TIME: 13:24:10	PRINT DATE: Tue Oct 12, 2004		
PATH: ADC\		ADC_ interlock.sch	

LOCAL/REMOTE WIRING DETAILS



MANUAL PADDLE

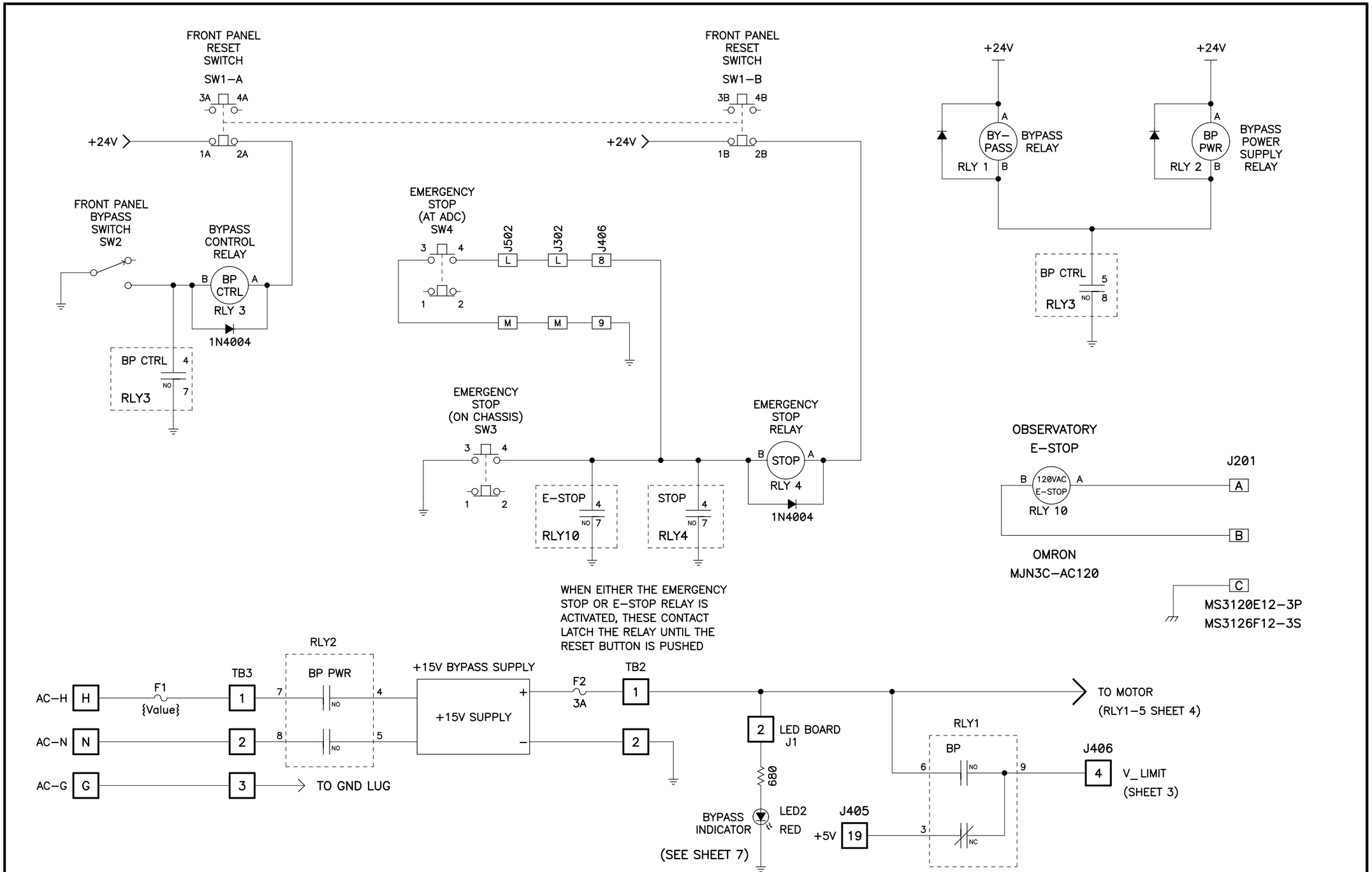
LOCAL/REMOTE CIRCUIT SHOWN HERE FOR CLARITY



REVISION

09-08-04 ADDED RELAY DESIGNATORS
10-12-04 ADDED LABEL (LED9) AND NOTE TO FRONT PANEL LED AND NO-NC LABELS TO RELAY CONTACTS
12-21-04 ADDED PWM BOARD BACK INTO THE SYSTEM

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		KECK ADC LIMIT INTERLOCK
DES'N BY: B. Alcott	ORIGIN DATE: 10-03-03	DWG. NO. EL-3612 NUM. 5 OF 8
Last SN	MODIFY DATE: 12-21-04	REV. B
PRINT TIME: 08:36:21	PRINT DATE: Tue Dec 21, 2004	
PATH: ADC\		ADC_interlock.sch

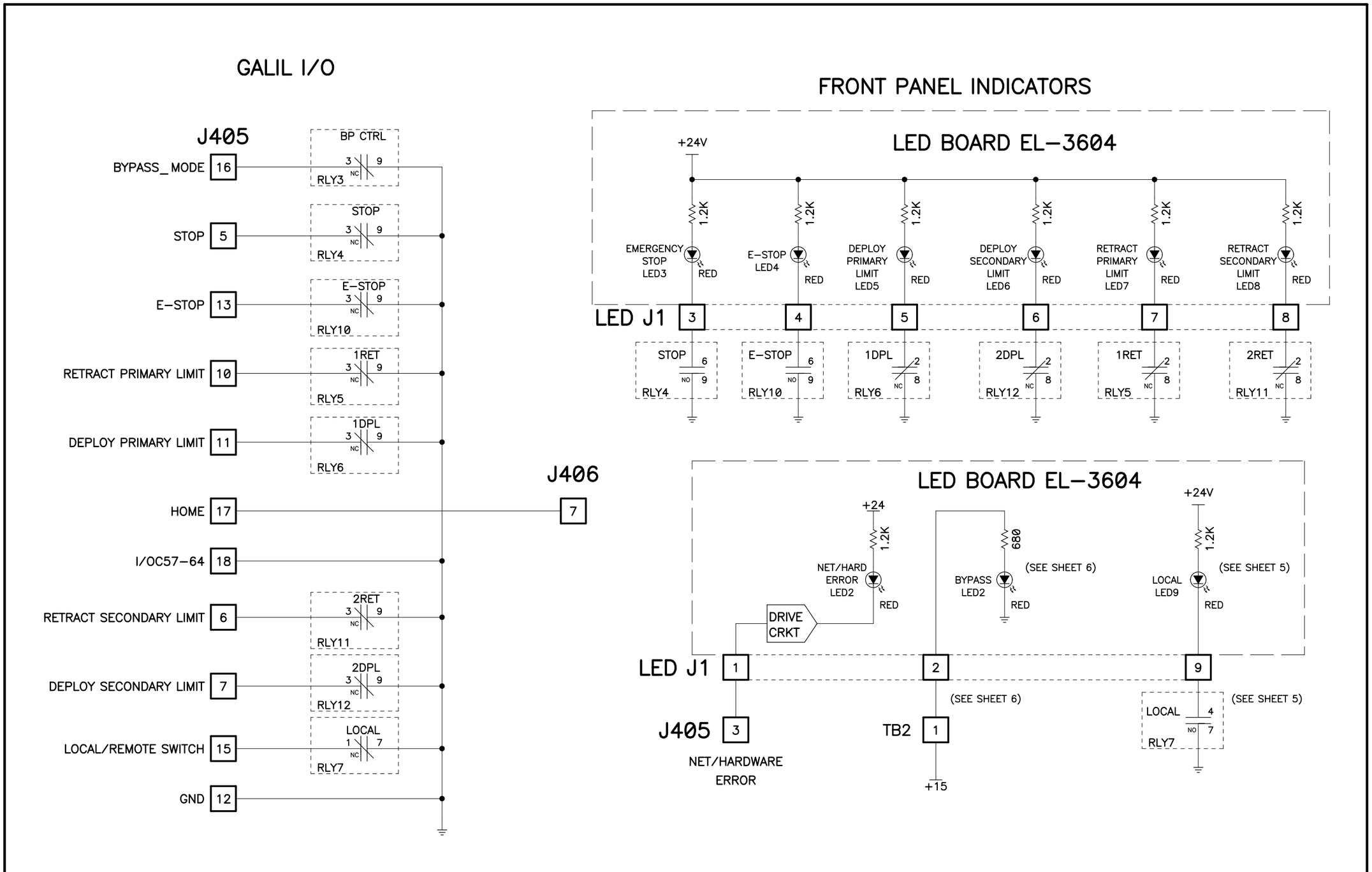


REVISION
09–08–04 ADDED RELAY DESIGNATORS
09–29–04 ADDED RELAY NUMBERS AND SWITCH NUMBERS
10–11–04 CORRECTED 15V SUPPLY AC WIRING
10–12–04 ADDED LABEL (LED2) AND NOTE TO BYPASS LED
10–12–04 ADDED NO & NC LABELS TO RELAY CONTACTS
10–25–04 ADDED TB2 TO +15V SUPPLY OUTPUT
10–29–04 ADDED 15 VOLT SUPPLY AC FUSE VALUE (1A) AND CORRECTED +5V PIN ON J405 FROM 2 TO 19.
01–21–05 CORRECTED GND PIN FOR STAGE EMERGENCY STOP SWITCH FROM 's' TO 'M'

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

KECK ADC
LIMIT INTERLOCK

DES'N BY: B. Alcott	ORIGIN DATE: 10–03–03	DWG. NO. EL–3612	NUM. 6 OF 8
Last SN	MODIFY DATE: 01–21–05		REV. B
PRINT TIME: 11:57:56	PRINT DATE: Fri Jan 21, 2005		
PATH: ADC\			ADC_interlock.sch



REVISION
06-22-04 ADDED J405 AND J406 PIN NUMBERS TO THIS SHEET
09-29-04 ADDED LOCAL/REMOTE SIGNALS AND ADDED RELAY NUMBERS
10-12-04 ADDED LED WIRING DETAILS
10-12-04 ADDED NO & NC LABELS TO RELAY CONTACTS
10-29-04 REMOVED INCORRECT CONNECTION FROM J406-8 TO GND
12-21-04 CHANGED FROM NO CONTACTS TO NC FOR STAGE LIMIT RELAY LED CONNECTIONS
02-07-05 CORRECTED NET/NETWORK LABEL TO NET/HARDWARE

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		KECK ADC LIMIT INTERLOCK	
DES'N BY: B. Alcott	ORIGIN DATE: 10-03-03	DWG. NO. EL-3612	NUM. 7 OF 8
Last SN	MODIFY DATE: 02-07-05		REV. B
PRINT TIME: 07:34:43	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC\		ADC_interlock.sch	

RELAY: RLY1 BYPASS

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	RLY8–4	RLY2–A	+24V	6
B	COIL–B	–	RLY2–B	BYPASS CONTROL SIGNAL	6
1	NC–1	–	RLY12–7	MOT1	4
2	NC–2	–	RLY7–9	MOT2	4
3	NC–3	–	J405–2	+5V	6
4	NO–1	RLY3–7	RLY7–7	GND	4
5	NO–2	–	RLY1–6	+15V	4
6	NO–3	RLY1–5	TB2–1	+15V	6
7	COM–1	J404–A	–	MOT1	4
8	COM–2	RLY11–1	–	MOT2	4
9	COM–3	J406–4	–	–	6

RELAY: RLY2 BP PWR

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	RLY1–A	TB1–1	+24V	6
B	COIL–B	RLY1–B	RLY3–5	BYPASS CONTROL SIGNAL	6
1	NC–1	–	–	–	–
2	NC–2	–	–	–	–
3	NC–3	J405–19	–	+5V	6
4	NO–1	AC FUSE	–	AC–H	6
5	NO–2	15V PS AC–N	–	–	6
6	NO–3	–	–	+15V	6
7	COM–1	–	TB3–1	AC–H	6
8	COM–2	–	TB3–2	AC–N	6
9	COM–3	–	J406–4	V_LIMIT	–

RELAY: RLY3 BP CTRL

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	–	SW1–2A	RESET	6
B	COIL–B	–	RLY3–4	BYPASS SWITCH	6
1	NC–1	–	–	–	–
2	NC–2	–	–	–	–
3	NC–3	J404–16	–	–	7
4	NO–1	RLY3–B	SW2–4	BYPASS SWITCH	6
5	NO–2	RLY2–B	–	BYPASS CONTROL SIGNAL	6
6	NO–3	–	–	–	–
7	COM–1	RLY1–4	RLY3–8	GND	6
8	COM–2	RLY3–7	RLY4–7	GND	6
9	COM–3	RLY10–9	RLY4–9	GND	7

RELAY: RLY4 STOP

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	–	SW1–2B	RESET	6
B	COIL–B	RLY10–4	RLY4–4	EMERGENCY STOP	6
1	NC–1	–	–	–	–
2	NC–2	RLY10–8	–	MOT2	4
3	NC–3	J405–5	–	–	7
4	NO–1	RLY4–B	SW3–4	EMERGENCY STOP	6
5	NO–2	–	–	–	–
6	NO–3	–	–	LED3	7
7	COM–1	RLY3–8	RLY5–B	GND	6
8	COM–2	RLY3–7	RLY11–7	GND	4
9	COM–3	RLY3–9	RLY5–8	GND	7

RELAY: RLY5 1RET

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	–	RLYBRD J2–3	1RET–DRV	3
B	COIL–B	RLY4–7	RLY6–B	GND	3
1	NC–1	–	–	–	–
2	NC–2	LED J1–7	–	LED7	7
3	NC–3	J405–10	–	1RET TO GALIL	7
4	NO–1	J202–C	–	DEPLOY_B	2
5	NO–2	–	–	–	–
6	NO–3	–	–	–	–
7	COM–1	–	RLY8–A	MDPL_OUT	2
8	COM–2	RLY4–9	RLY5–9	GND	7
9	COM–3	RLY5–8	RLY6–8	GND	7

RELAY: RLY6 1DPL

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	–	RLYBRD J2–4	1DPL_DRV	3
B	COIL–B	RLY5–B	TB1–5	GND	3
1	NC–1	–	–	–	–
2	NC–2	LED J1–5	–	LED5	7
3	NC–3	J405–11	–	1DPL TO GALIL	7
4	NO–1	–	RLY9–A	RETRACT+	2
5	NO–2	–	–	–	–
6	NO–3	–	–	–	–
7	COM–1	J202–D	–	RETRACT_A	2
8	COM–2	RLY5–9	RLY6–9	GND	7
9	COM–3	RLY6–8	TB1–4	GND	7

RELAY: RLY7 LOCAL

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	J202–G	–	$\overline{\text{LOCAL}}$/REMOTE SWITCH	2, 5
B	COIL–B	–	RLY8–1	GND	2, 5
1	NC–1	J405–15	–	$\overline{\text{LOCAL}}$/REMOTE TO GALIL	5, 7
2	NC–2	–	J403–A	MOT1–IN	5
3	NC–3	–	J403–B	MOT2–IN	5
4	NO–1	–	LED–A	FRONT PANEL LOCAL LED9	5, 7
5	NO–2	–	RLY8–7	MANUAL DEPLOY	5
6	NO–3	–	RLY9–7	MANUAL RETRACT	5
7	COM–1	RLY1–4	–	GND	5, 7
8	COM–2	RLY12–1	–	MOT1	5
9	COM–3	RLY1–2	–	MOT2	5

RELAY: RLY8 MDPL

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	RLY5–7	–	MDEPLOY+	2
B	COIL–B	J202–B	–	DEPLOY_A	2
1	NC–1	RLY7–B	RLY9–1	GND	5
2	NC–2	–	–	–	–
3	NC–3	–	–	–	–
4	NO–1	RLY9–4	RLY1–A	+24V	5
5	NO–2	–	–	–	–
6	NO–3	–	–	–	–
7	COM–1	RLY7–5	–	MANUAL DEPLOY	5
8	COM–2	–	–	–	–
9	COM–3	–	–	–	–

RELAY: RLY9 MRET

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	RLY6–1	–	MRETRACT+	2
B	COIL–B	J202–E	–	RETRACT_B	2
1	NC–1	RLY8–1	RLY10–7	GND	5
2	NC–2	–	–	–	–
3	NC–3	–	–	–	–
4	NO–1	–	RLY8–4	+24V	5
5	NO–2	–	–	–	–
6	NO–3	–	–	–	–
7	COM–1	RLY7–6	–	MANUAL RETRACT	5
8	COM–2	–	–	–	–
9	COM–3	–	–	–	–

RELAY: RLY10 E–STOP

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	J201–A	–	OBSERVATORY E–STOP (AC)	6
B	COIL–B	J202–B	–	OBSERVATORY E–STOP (AC)	6
1	NC–1	–	–	–	–
2	NC–2	J404–B	–	MOT2	4
3	NC–3	J405–13	–	–	7
4	NO–1	J406–8	RLY4–B	E–STOP	6
5	NO–2	–	–	–	–
6	NO–3	–	–	LED4	7
7	COM–1	RLY9–1	RLY11–B	GND	6
8	COM–2	–	RLY4–2	MOT2	4
9	COM–3	RLY11–8	RLY3–9	GND	7

RELAY: RLY11 2RET

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	–	RLYBRD J2–1	3RET_DRV	3
B	COIL–B	RLY10–7	–	GND	3
1	NC–1	–	–	–	–
2	NC–2	LED J1–8	–	LED8	7
3	NC–3	J405–6	–	2RET TO GALIL	7
4	NO–1	–	RLY1–8	MOT2	4
5	NO–2	–	–	–	–
6	NO–3	–	–	–	–
7	COM–1	RLY4–8	–	MOT2	4
8	COM–2	RLY11–9	RLY10–9	GND	7
9	COM–3	RLY12–8	RLY11–8	GND	7

RELAY: RLY12 2DPL

PIN	CONTACT	FROM	TO	SIGNAL	SHEETS
A	COIL–A	–	RLYBRD J2–2	2DPL_DRV	3
B	COIL–B	RLY11–B	TB1–6	–	3
1	NC–1	–	–	–	–
2	NC–2	LED J1–6	–	LED6	7
3	NC–3	J405–7	–	2DPL TO GALIL	7
4	NO–1	–	RLY7–8	MOT1	4
5	NO–2	–	–	–	–
6	NO–3	–	–	–	–
7	COM–1	RLY1–1	–	MOT1	4
8	COM–2	RLY12–9	RLY11–9	GND	7
9	COM–3	–	RLY12–8	GND	7

REVISION

10–12–04 ADDED DETAILS
10–25–04 CORRECTED RLY2–3, RLY10–3, RLY11–3, AND RLY12–3 'FROM' LABELS
12–21–04 CHANGED FROM NO CONTACTS TO NC FOR STAGE LIMIT RELAY LED CONNECTIONS
01–05–05 SWAPPED LIMIT SENSE FOR BYPASS MODE AND MANUAL MODE TO MAKE MANUAL OPERATION MOVE THE MOTOR THE SAME DIRECTION

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	KECK ADC LIMIT INTERLOCK
DES'N BY: B. Alcott	ORIGIN DATE: 10–03–03
Last SN	MODIFY DATE: 01–05–05
PRINT TIME: 12:30:37	PRINT DATE: Fri Jan 21, 2005
PATH: ADC\	
DWG. NO. EL–3612	NUM. 8 OF 8
REV. B	
ADC_interlock.sch	

E–STOP (J201)

BOX MOUNT: MS3122E12–3P
STRAIGHT PLUG: MS3126F12–3S

POWER ENTRY MODULE

PIN	TO	SIGNAL	FUNCTION
A	–	AC–H	AC POWER HOT
B	–	AC–N	AC POWER NEUTRAL
C	–	GND	GND

+24V SUPPLY (J402)

BOX MOUNT: MS3122E8–3P
STRAIGHT PLUG: MS3126F8–3S

MS CONNECTOR 8–3 INSERT

PIN	TO	SIGNAL	FUNCTION
A	SERVO SUPPLY +	+24V	+24V
B	SERVO SUPPLY –	+24V RTN	GND
C	SERVO SUPPLY –	+24V RTN	GND

MANUAL CONTROL PADDLE CABLE (J202)

BOX MOUNT: MS3122E16–8S
STRAIGHT PLUG: MS3126E16–8P

MS CONNECTOR 16–8 INSERT

PIN	TO	SIGNAL	FUNCTION
A	–	+24V	+24V
B	–	DEPLOY_A	FROM DEPLOY PUSHBUTTON
C	–	DEPLOY_B	FROM DEPLOY PUSHBUTTON
D	–	RETRACT_A	FROM RETRACT PUSHBUTTON
E	–	RETRACT_B	FROM RETRACT PUSHBUTTON
F	–	$\overline{\text{MAN_PADDLE_CONN}}$	LOW WHEN PADDLE CONNECTED
G	–	$\overline{\text{LOCAL/REMOTE}}$	LOW WHEN LOCAL IS SELECTED
H	–	GND	24V RETURN

MOTOR DRIVE IN (J403)

BOX MOUNT: MS3122E14–5P
STRAIGHT PLUG: MS3126F14–5S

MS CONNECTOR 14–5 INSERT

PIN	TO	SIGNAL	FUNCTION
A	AMP X–AXIS PIN 2	MOT1	MOTOR POWER
B	AMP X–AXIS PIN 4	MOT2	MOTOR POWER
C	J403–C	$\overline{\text{MOTOR_CONN}}$	MOTOR CABLE CONNECTED OUT
D	IOM–20	$\overline{\text{MOTOR_CONN}}$	MOTOR CABLE CONNECTED IN
E	–	–	–

AC POWER (J401)

POWER ENTRY MODULE

PIN	TO	SIGNAL	FUNCTION
A	PULIZZI CH. 3	AC–H	AC POWER HOT
B	PULIZZI CH. 3	AC–N	AC POWER NEUTRAL
C	PULIZZI CH. 3	GND	GND

MOTOR DRIVE OUT (J404)

BOX MOUNT: MS3122E14–5S
STRAIGHT PLUG: MS3126F14–5P

MS CONNECTOR 14–5 INSERT

PIN	TO	SIGNAL	FUNCTION
A	J301–A	MOT1	MOTOR POWER
B	J301–B	MOT2	MOTOR POWER
C	J301–C	$\overline{\text{MOTOR_CONN}}$	MOTOR CABLE CONNECTED SIGNAL
D	J301–D	GND	GND
E	J301–E	–	–

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_interlock_cables_SH1.sch.pdf

04–28–04 ADDED CONNECTOR PART NUMBERS
05–06–04 CORRECTED SENSE OF SIGNALS FROM HALL–EFFECT SWITCHES – NOW, BLOCKED = HIGH
06–14–04 REMOVED EMERGENCY NULL PADDLE AND ADDED LOCAL/REMOTE PADDLE TO J406
06–21–04 CORRECTED PIN OUT FOR J404

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		KECK ADC INTERLOCK CABLES	
DES'N BY: B. Alcott	ORIGIN DATE: 04–22–04	DWG. NO. EL–3613	NUM. 1 OF 2
Last SN	MODIFY DATE: 06–21–04		REV. A
PRINT TIME: 09:24:59	PRINT DATE: Wed Sep 08, 2004		
PATH: ADC\		ADC_interlock_cables.sch	

NUM. 1 OF 2

KECK ADC INTERLOCK CABLES

EL–3613

GENERAL I/O TO GALIL (J405)

CHASSIS MOUNT: DB25P
CABLE END: DB25S

PIN	BIT	TO	SIGNAL	FUNCTION
1	–	J701–1	GND	GND
2	–	J701–2	–	–
3	33	J701–3	$\overline{\text{NET/HARDWARE_ERR}}$	NET/HARDWARE ERROR LED
4	–	J701–4	GND	GND – STOP, ESTOP, LOCAL/REMOTE, BYPASS
5	66	J701–5	$\overline{\text{EMERGENCY_STOP}}$	EMERGENCY STOP SIGNAL
6	49	J701–6	2RET	FWD CELL RETRACT SECONDARY LIM
7	50	J701–7	2DPL	FWD CELL DEPLOY SECONDARY LIM
8	57	J701–8	$\overline{\text{MOTOR_CONN}}$	MOTOR CABLE CONNECTED
9	62	J701–9	$\overline{\text{MAN_PADDLE_CONN}}$	LOW WHEN PADDLE IS CONNECTED
10	REV	J3–11	1RET	RETRACT PRIMARY LIMIT
11	FWD	J3–41	1DPL	DEPLOY PRIMARY LIMIT
12	–	J701–10	GND	GND – CONNECTOR LINES
13	65	J701–11	$\overline{\text{E–STOP}}$	OBSERVATORY E–STOP SIGNAL
14	–	–	–	–
15	67	J701–12	$\overline{\text{LOCAL/REMOTE}}$	COMPUTER/REMOTE CONTROL SIGNAL
16	68	J701–13	BYPASS_MODE	EMERGENCY NULL SIGNAL
17	HOME	J3–26	HOME	HOME FIDUCIAL SIGNAL
18	–	J3–34	GND	GND – HOME SENSOR
19	–	J3–32	+5V	+5V – HOME SENSOR
20	–	J701–14	GND	GND – SECONDARY LIMITS
21	–	J701–15	GND	GND – NET/HARD ERROR
22	–	–	–	–
23	–	–	–	–
24	–	–	–	–
25	–	–	–	–

GENERAL I/O FROM STAGE (J406)

CHASSIS MOUNT: DB15S
CABLE END: DB15P

PIN	TO	SIGNAL	FUNCTION
1	J302–p	GND	GND
2	J302–t	FWD_RET_2ND	RETRACT SECONDARY LIMIT
3	J302–u	FWD_DEP_2ND	DEPLOY SECONDARY LIMIT
4	J302–r	V_LIMIT	HALL EFFECT SENSOR POWER
5	J302–P	REV_LIM	RETRACT PRIMARY LIMIT
6	J302–U	FWD_LIM	DEPLOY PRIMARY LIMIT
7	J302–R	HOME	HOME FIDUCIAL SIGNAL
8	J302–L	SW4–4	EMERGENCY STOP
9	J302–M	SW4–3	GND (EMERGENCY STOP)
10	–	–	–
11	–	–	–
12	–	–	–
13	–	–	–
14	–	–	–
15	–	–	–

REVISIONS

http://loel.ucolick.org/manual/ADC/schematics/ADC_interlock_cables_SH2.sch.pdf

04–26–04 CHANGED FROM DB15 AND DB9 TO DB25 AND DB15 – NEEDED 10 PINS FOR J006
05–06–04 CORRECTED SENSE OF SIGNALS FROM HALL–EFFECT SWITCHES – NOW, BLOCKED = HIGH
06–14–04 REMOVED EMERGENCY NULL PADDLE AND ADDED LOCAL/REMOTE PADDLE TO J406
09–08–04 ADDED COMMON FOR NET/HARD ERROR AT J405–21 AND SIGNAL DETAILS ON J405 PINS 4, 12,19–21
09–25–04 CORRECTED GND PINS AND REMOVE +5V AT PIN 2 (USES PIN 19 5V).
02–07–05 CORRECTED NET/HARD ERROR I/O PIN FROM IOM–PIN 60 TO IOM–PIN 62 AND ADDED J701 CONNECTIONS

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

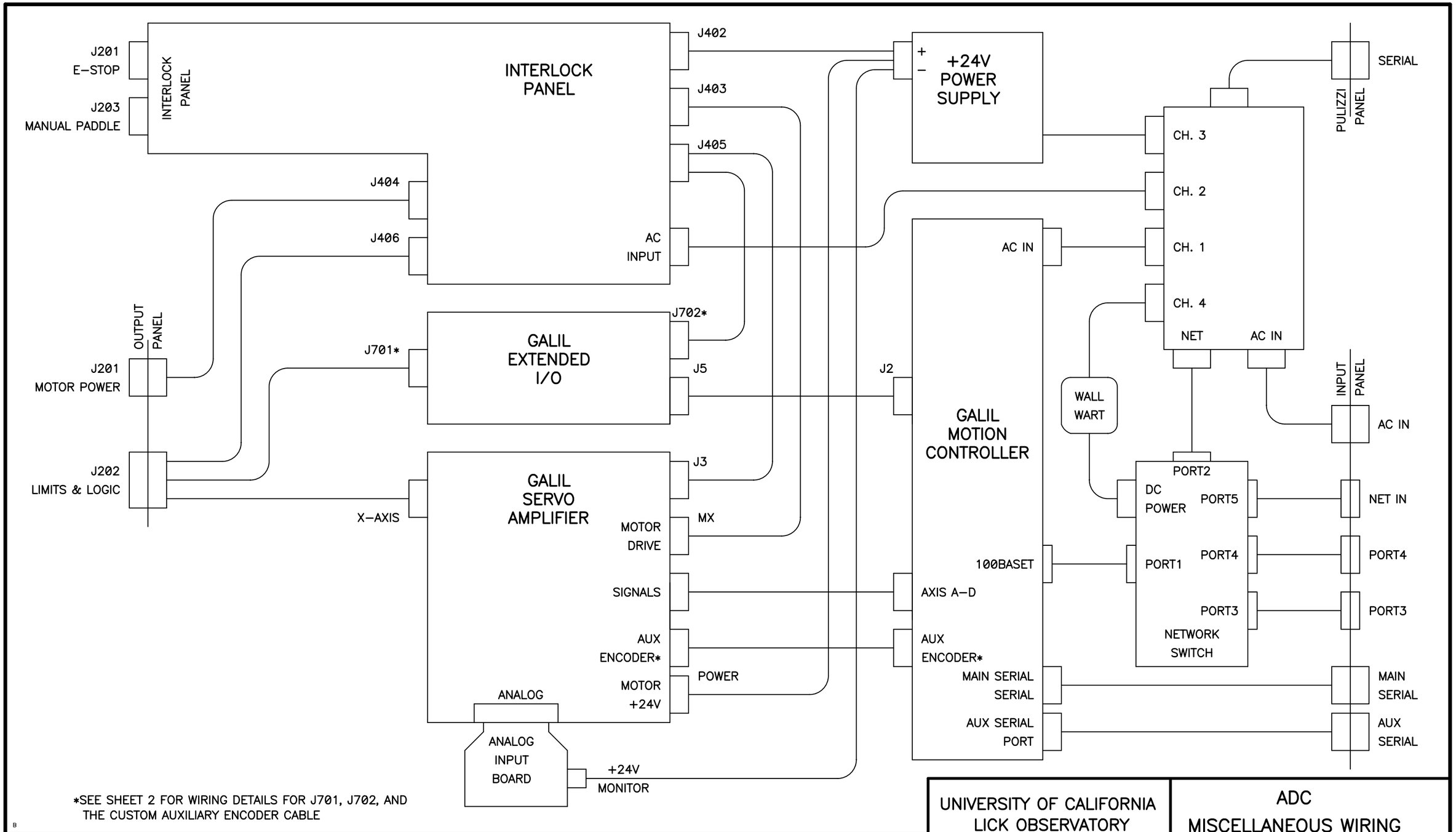
KECK ADC
INTERLOCK CABLES

DES'N BY: B. Alcott	ORIGIN DATE: 04–22–04	DWG. NO.	NUM. 2 OF 2
Last SN	MODIFY DATE: 02–07–05	EL–3613	REV. A
PRINT TIME: 07:35:22	PRINT DATE: Wed Mar 23, 2005		
PATH: ADC\		ADC_interlock_cables.sch	

NUM. 2 OF 2

KECK ADC INTERLOCK CABLES

EL–3613



*SEE SHEET 2 FOR WIRING DETAILS FOR J701, J702, AND THE CUSTOM AUXILIARY ENCODER CABLE

B

REVISIONS

04-12-05 CLEANED UP AND ADDED SOME LABELS

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	ADC MISCELLANEOUS WIRING

DES'N BY: B. Alcott	ORIGIN DATE: 01-04-05	DWG. NO. EL-3614	NUM. 1 OF 2
Last SN	MODIFY DATE: 04-13-05		REV. A
PRINT TIME: 09:26:13	PRINT DATE: Wed Apr 13, 2005		
PATH: ADC/		ADC_misc_wiring.SCH	

NUM. 1 OF 2

ADC MISCELLANEOUS WIRING

EL-3614

DB-25 CONNECTOR J701 ON THE GALIL EXTENDED I/O PANEL

J701	TO	SIGNAL
1	J202-A	GND
2	J202-B	$\overline{\text{MAIN_CABLE_CONN}}$
3	N/C	–
4	N/C	–
5	N/C	–
6	N/C	–
7	J202-N	GND
8	J202-S	+5V
9	J202-T	GND
10	J202-v	AFT_RET_2ND
11	J202-w	AFT_DEP_2ND
12	J202-x	AFT_HOME
13	J202-y	GND
14	N/C	–
15	J202-AA	$\overline{\text{MOTOR_ENCD_CONN}}$
16	J202-BB	$\overline{\text{LOAD_ENCD_CONN}}$
17	J202-CC	$\overline{\text{FWD_CELL_CONN}}$
18	J202-DD	$\overline{\text{AFT_CELL_CONN}}$
19	N/C	–
20	N/C	–
21	N/C	–
22	N/C	–
23	N/C	–
24	N/C	–
25	N/C	–

DB-15HD CONNECTOR J702 ON THE GALIL EXTENDED I/O PANEL

J702	TO	SIGNAL
1	J405-1	GND
2	J405-2	(NOT USED)
3	J405-3	$\overline{\text{NET/HARDWARE_ERR}}$
4	J405-4	GND
5	J405-5	$\overline{\text{EMERGENCY_STOP}}$
6	J405-6	2RET
7	J405-7	2DPL
8	J405-8	$\overline{\text{MOTOR_CONN}}$
9	J405-9	$\overline{\text{MAN_PADDLE_CONN}}$
10	J405-12	GND
11	J405-13	$\overline{\text{E-STOP}}$
12	J405-15	$\overline{\text{LOCAL}}$/REMOTE
13	J405-16	BYPASS_MODE
14	J405-20	GND
15	J405-21	GND

CABLE FROM GALIL DMC-2210 TO AMP-19240 CONNECTES AUXILIARY ENCODER

36-PIN	DB-25	SIGNAL	COLOR
1	1	+5V	BLK
2	14	GND	BRN
3	2	AA+X	RED
4	15	AA-X	ORN
5	3	AB+X	YEL
6	16	AB-X	GRN
19	N/C	+5V	BLK/WHT
20	19	GND	BRN/WHT

THIS IS A GALIL 36-PIN CABLE THAT HAS BEEN CUT TO SIZE AND THEN TERMINATED INTO A DB25 CONNECTOR. (A SPARE TESTED CABLE HAS BEEN INCLUDED WITH THE INSTRUMENT)

REVISION

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

ADC MISCELLANEOUS WIRING

DES'N BY: B. Alcott	ORIGIN DATE: 01-04-05	DWG. NO.	NUM. OF 2
Last SN	MODIFY DATE:	EL-3614	REV. A
PRINT TIME: 07:43:55	PRINT DATE: Wed Mar 23, 2005		
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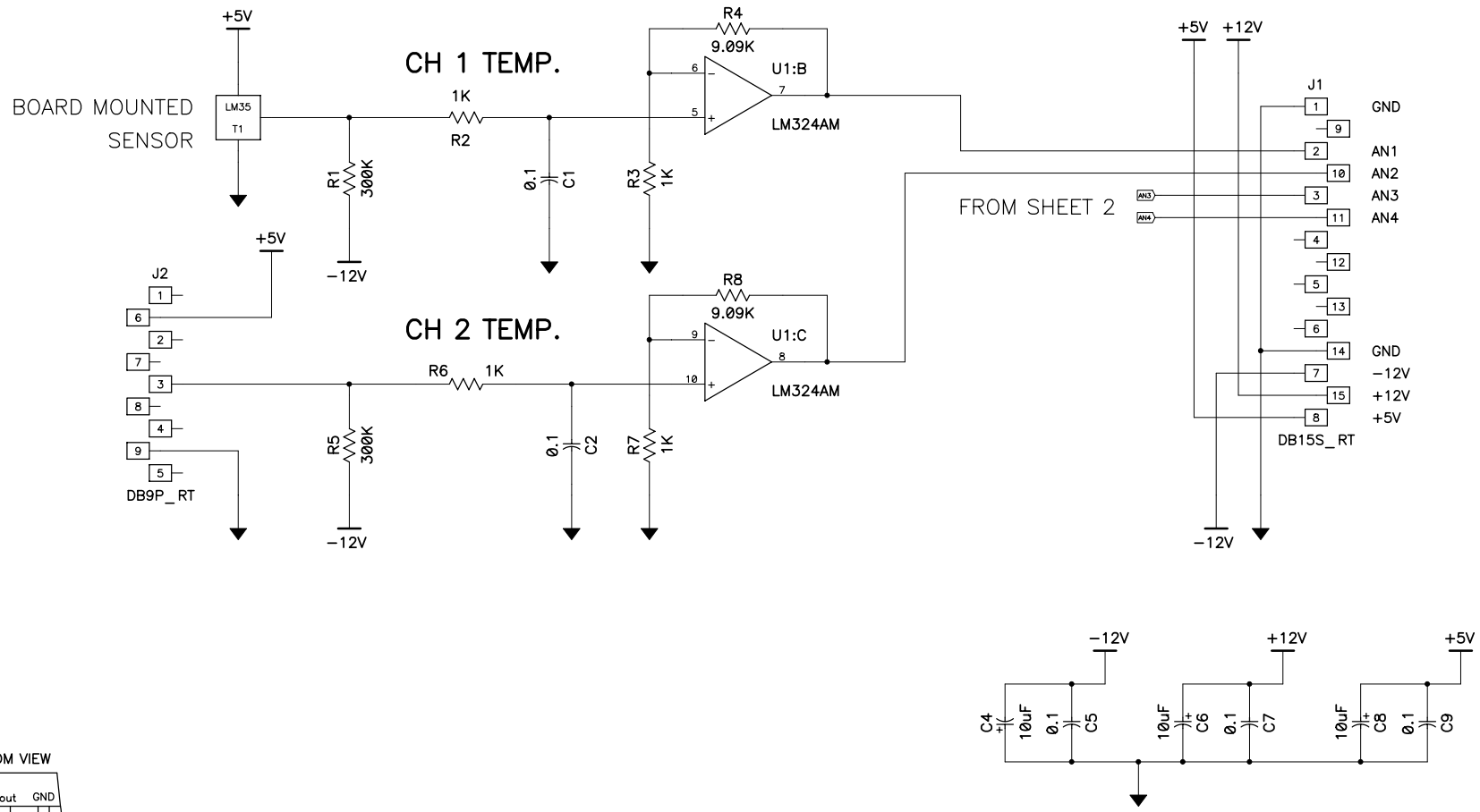

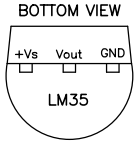

REVISIONS

04-14-04 CHANGED BOARD NAME TO 4 CHANNEL FROM 3 CHANNEL
11-24-04 ADDED LABEL FOR 4TH ANALOG SIGNAL (AN4)

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	4 CHANNEL TEMPERATURE SENSOR BOARD

DES'N BY: B. Alcott	ORIGIN DATE: 03-17-04	DWG. NO. EL-1356	NUM. 1 OF 2
Last SN	MODIFY DATE: 11-24-04		REV. A
PRINT TIME: 08:17:49	PRINT DATE: Wed Nov 24, 2004		
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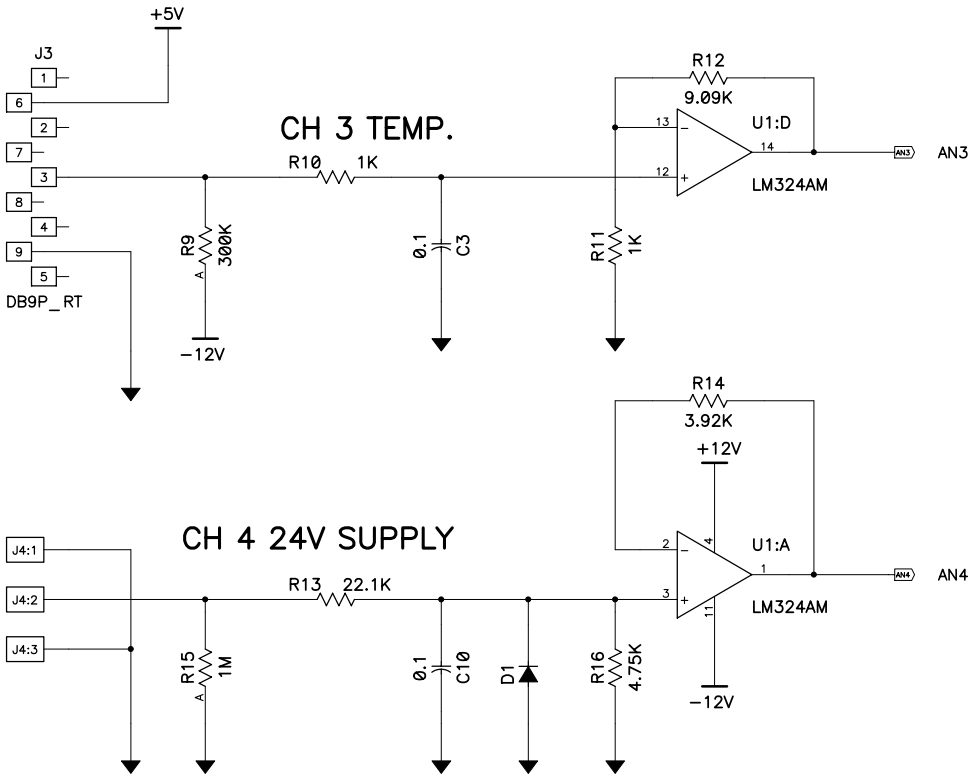
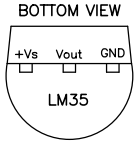
NUM. 1 OF 2

4 CHANNEL TEMPERATURE SENSOR BOARD

EL-1356





B

REVISIONS

04-14-04 CHANGED BOARD NAME TO 4 CHANNEL FROM 3 CHANNEL

UNIVERSITY OF CALIFORNIA LICK OBSERVATORY	4 CHANNEL TEMPERATURE SENSOR BOARD

DES'N BY: B. Alcott	ORIGIN DATE: 03-17-04	DWG. NO. EL-1356	NUM. 2 OF 2
Last SN	MODIFY DATE: 04-14-04		REV. A
PRINT TIME: 08:18:00	PRINT DATE: Wed Nov 24, 2004		
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NUM. 2 OF 2

4 CHANNEL TEMPERATURE SENSOR BOARD

EL-1356